

Fig. 1

2168

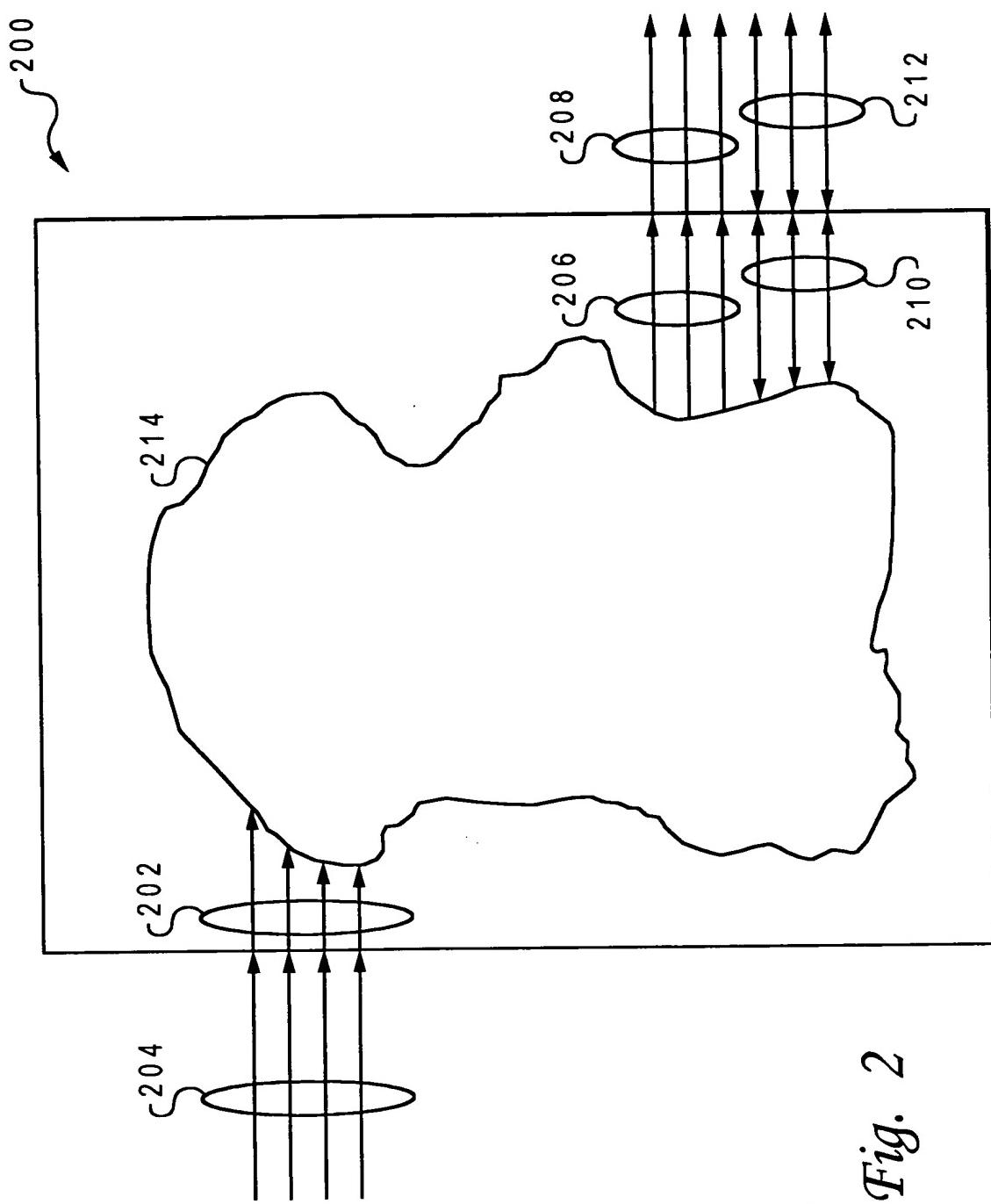
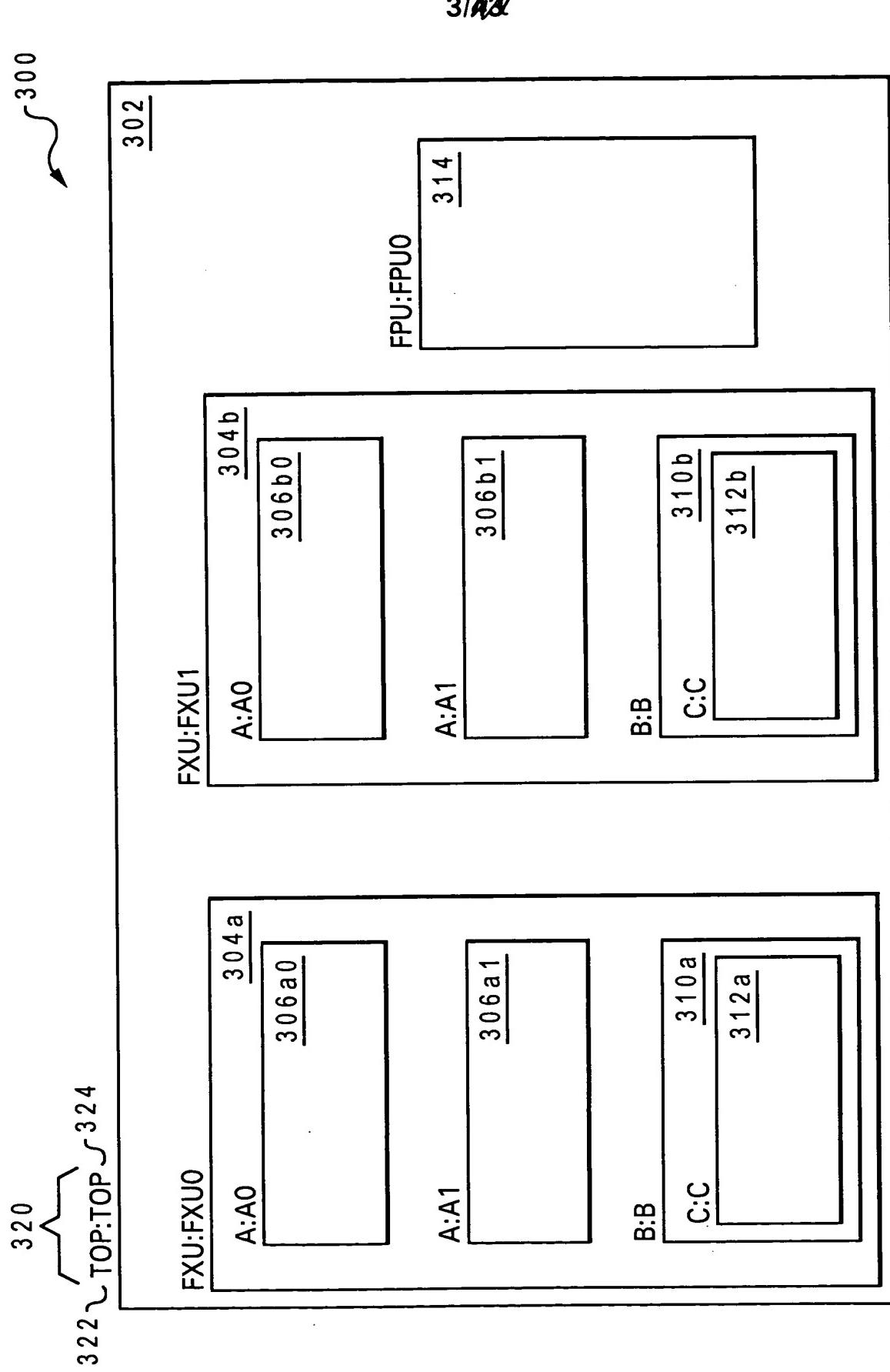


Fig. 2

Fig. 3



400

```
ENTITY A IS
  PORT
  (
    ...
    );
END A

ARCHITECTURE A OF A IS
...
BEGIN
...
--## statementA
--## statementB
--## statementC
...
--## statementD
--## statementE
--## statementF
...
END;
```

402 -- port_list

404 -- signal declarations

406 -- HDL code describing design

408 -- HDL code describing design

410 -- HDL code describing design

Fig. 4A

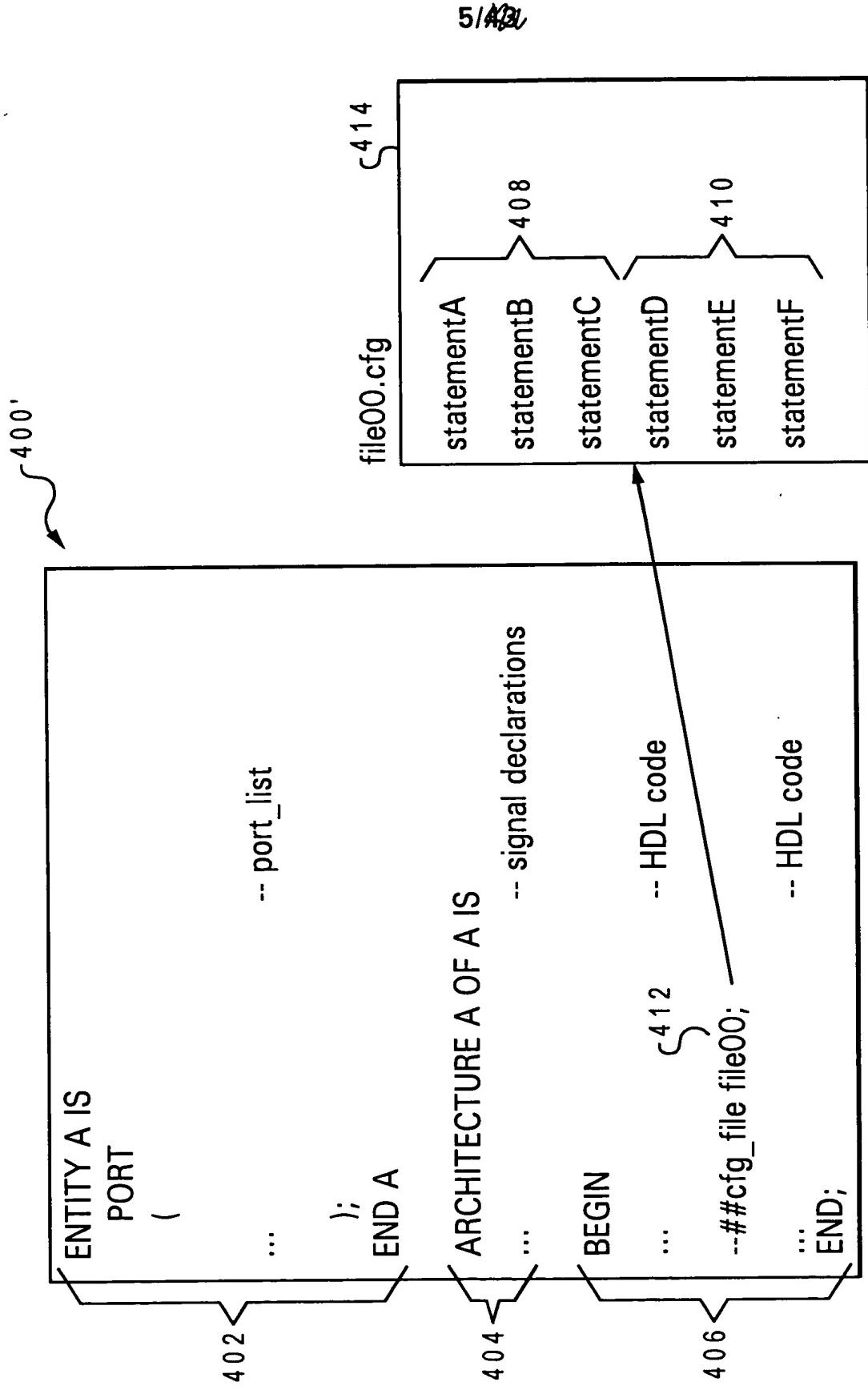


Fig. 4B

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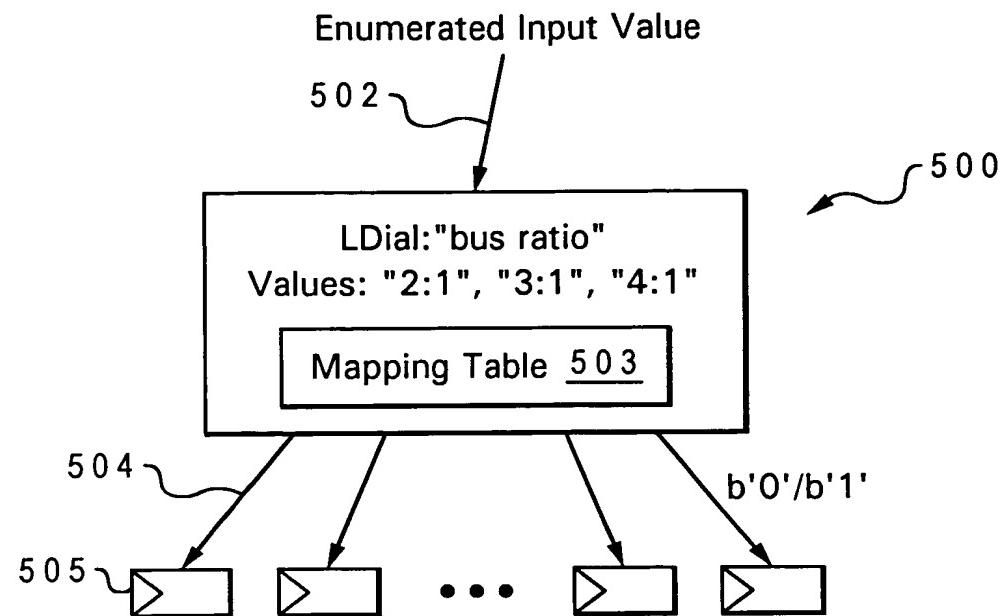


Fig. 5A

Enumerated Input Value: "ON" or "OFF"

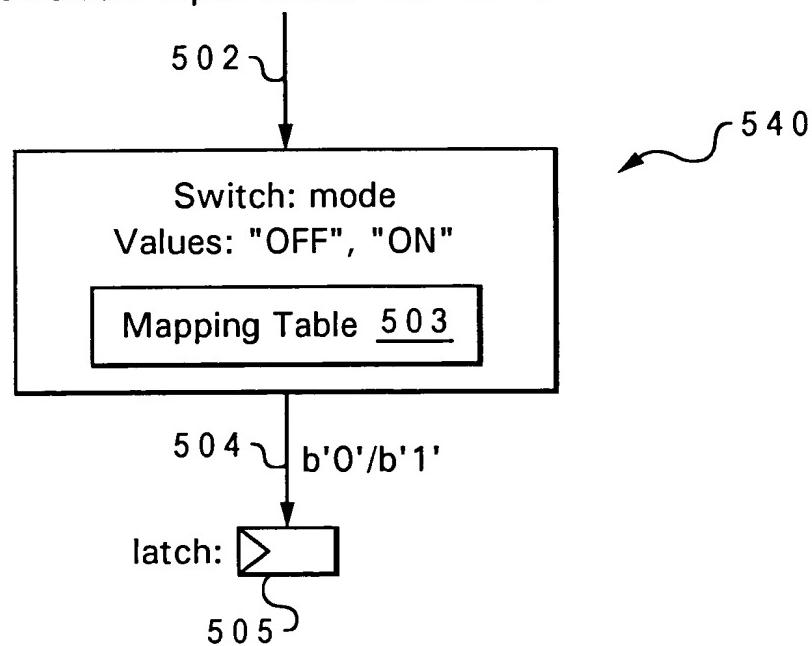
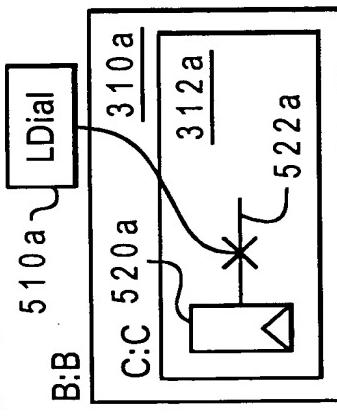
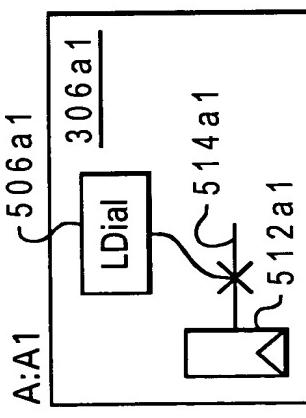
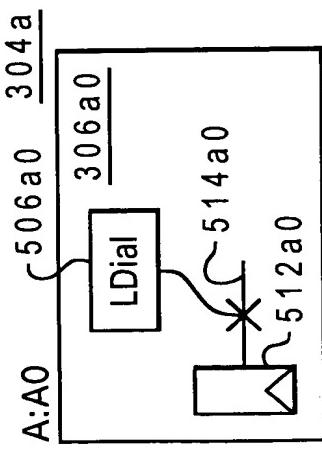


Fig. 5D

TOP:TOP

FXU:FXU0

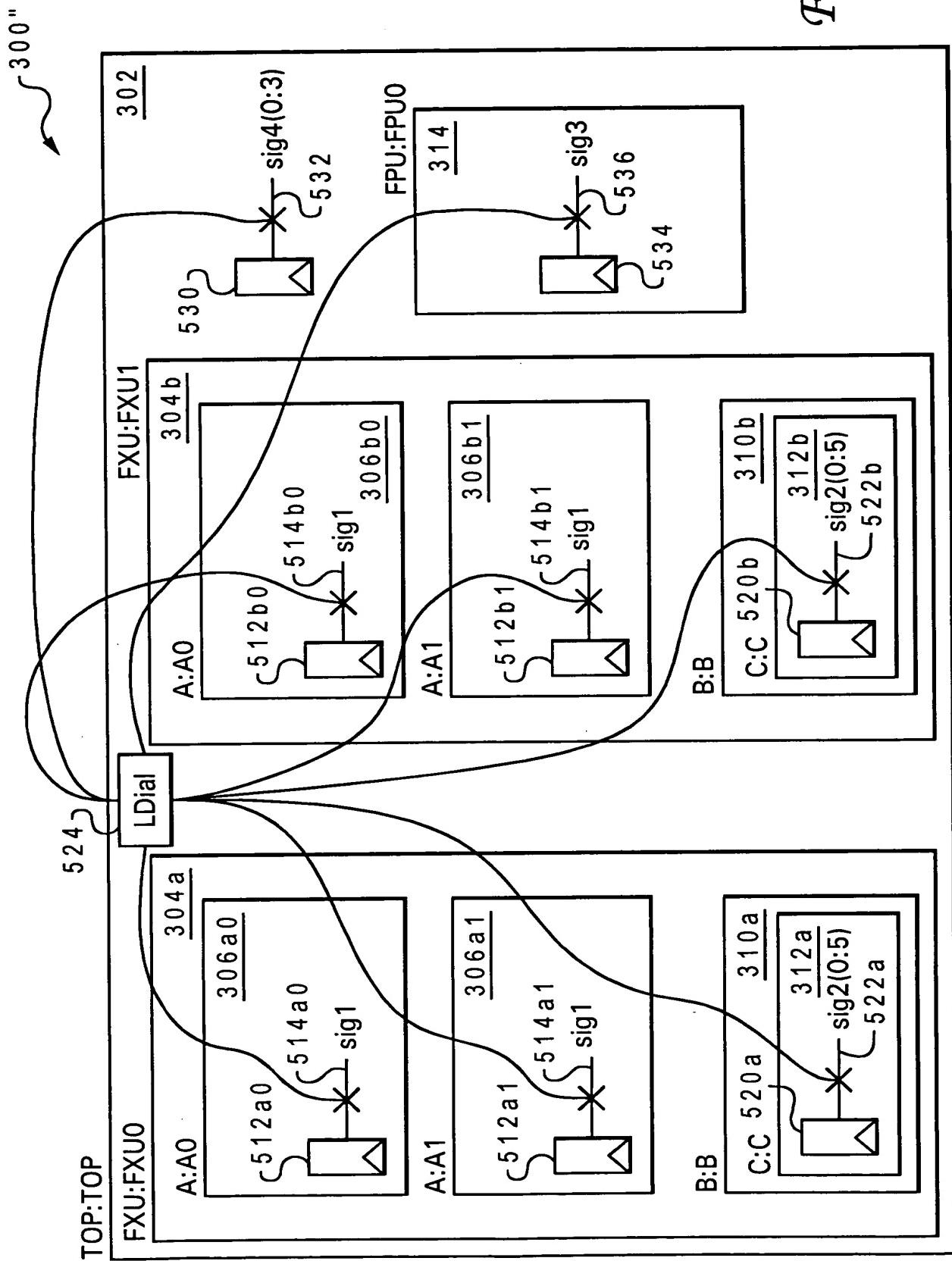


300'

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Fig. 5B

Fig. 5C



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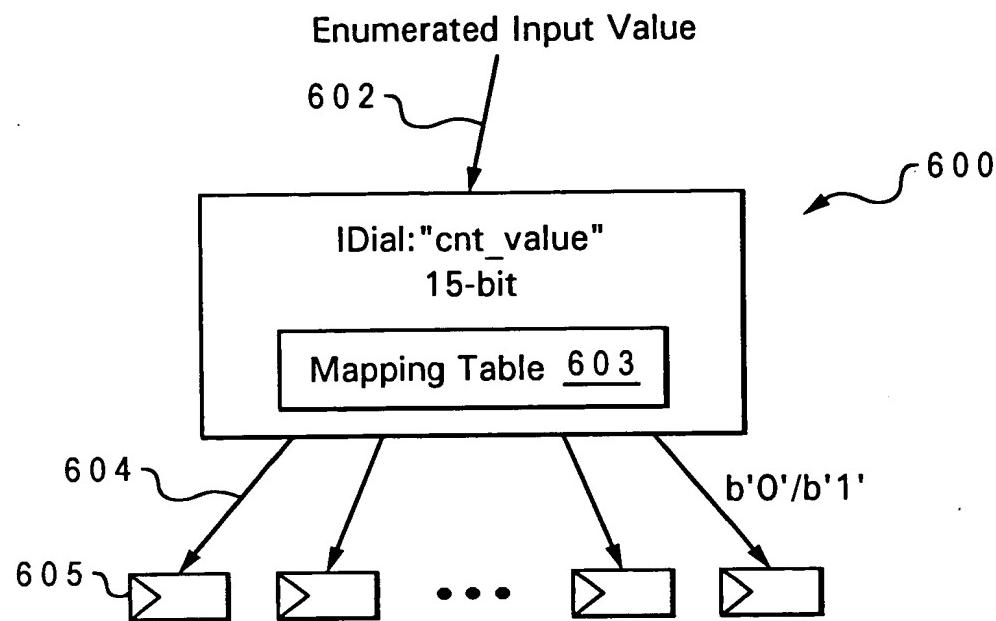


Fig. 6A

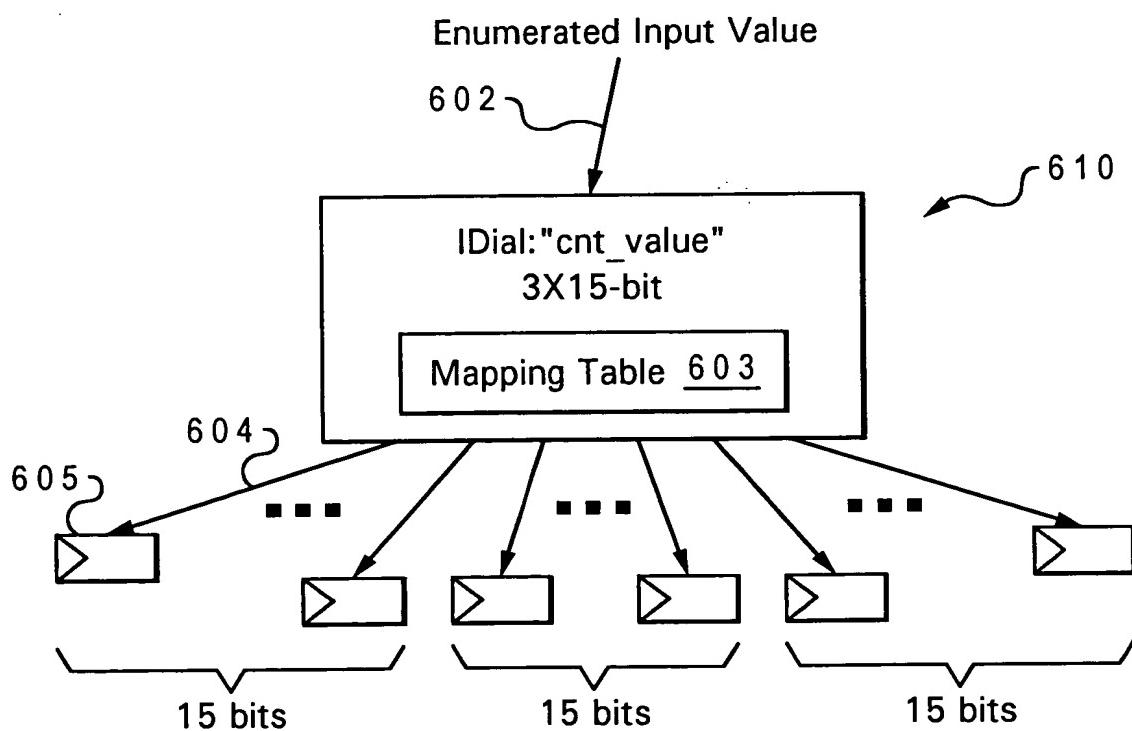


Fig. 6B

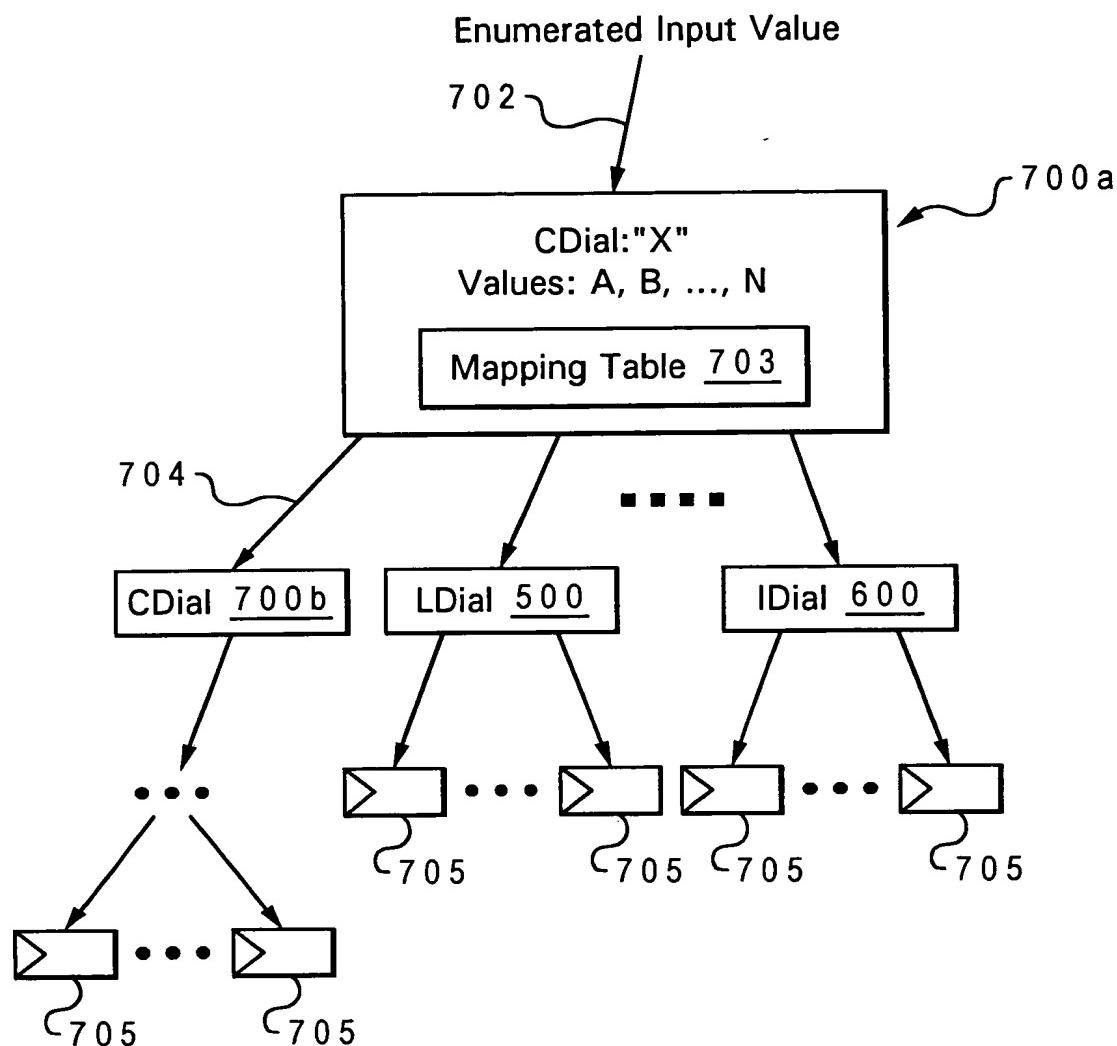
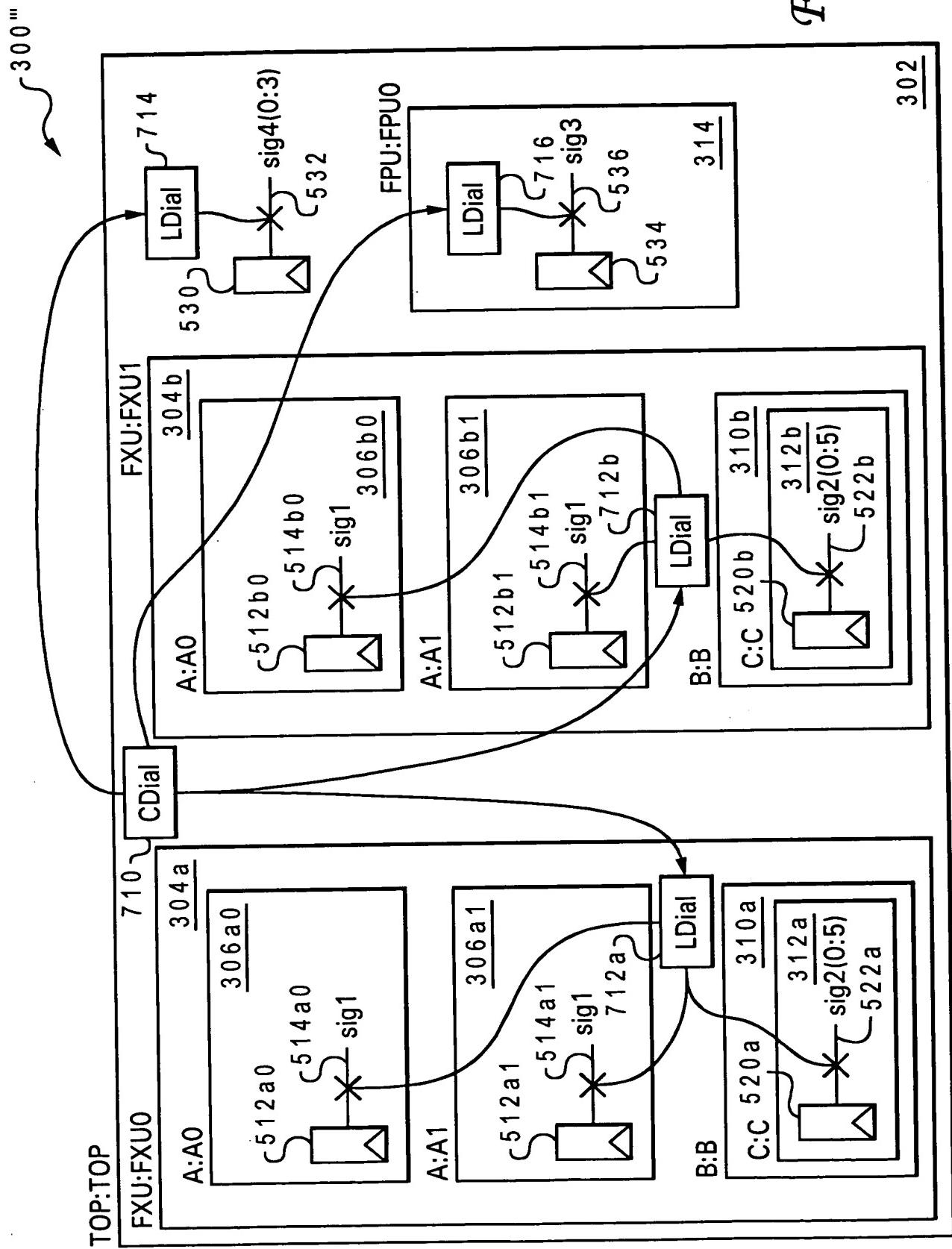


Fig. 7A

Fig. 7B



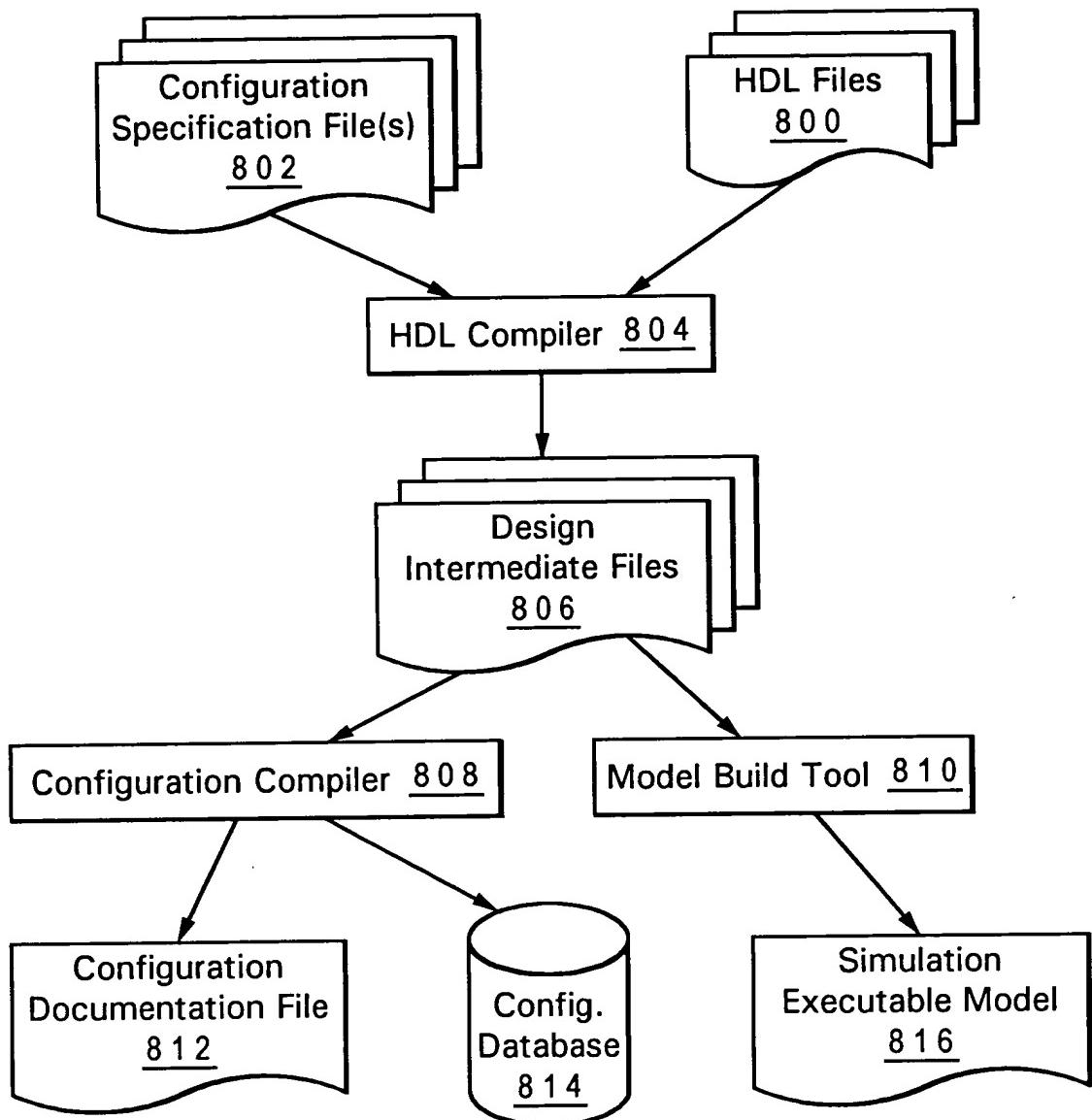


Fig. 8

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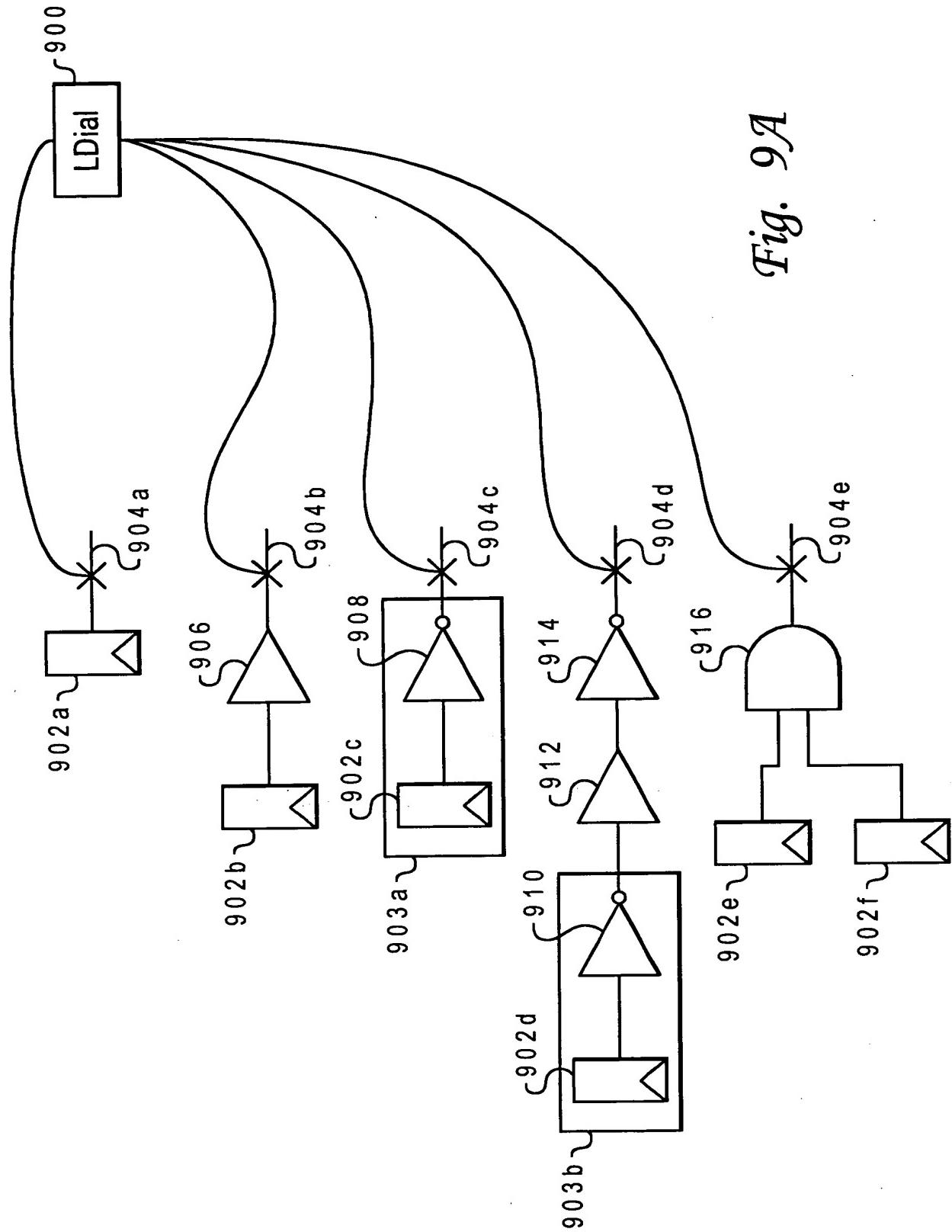


Fig. 9A

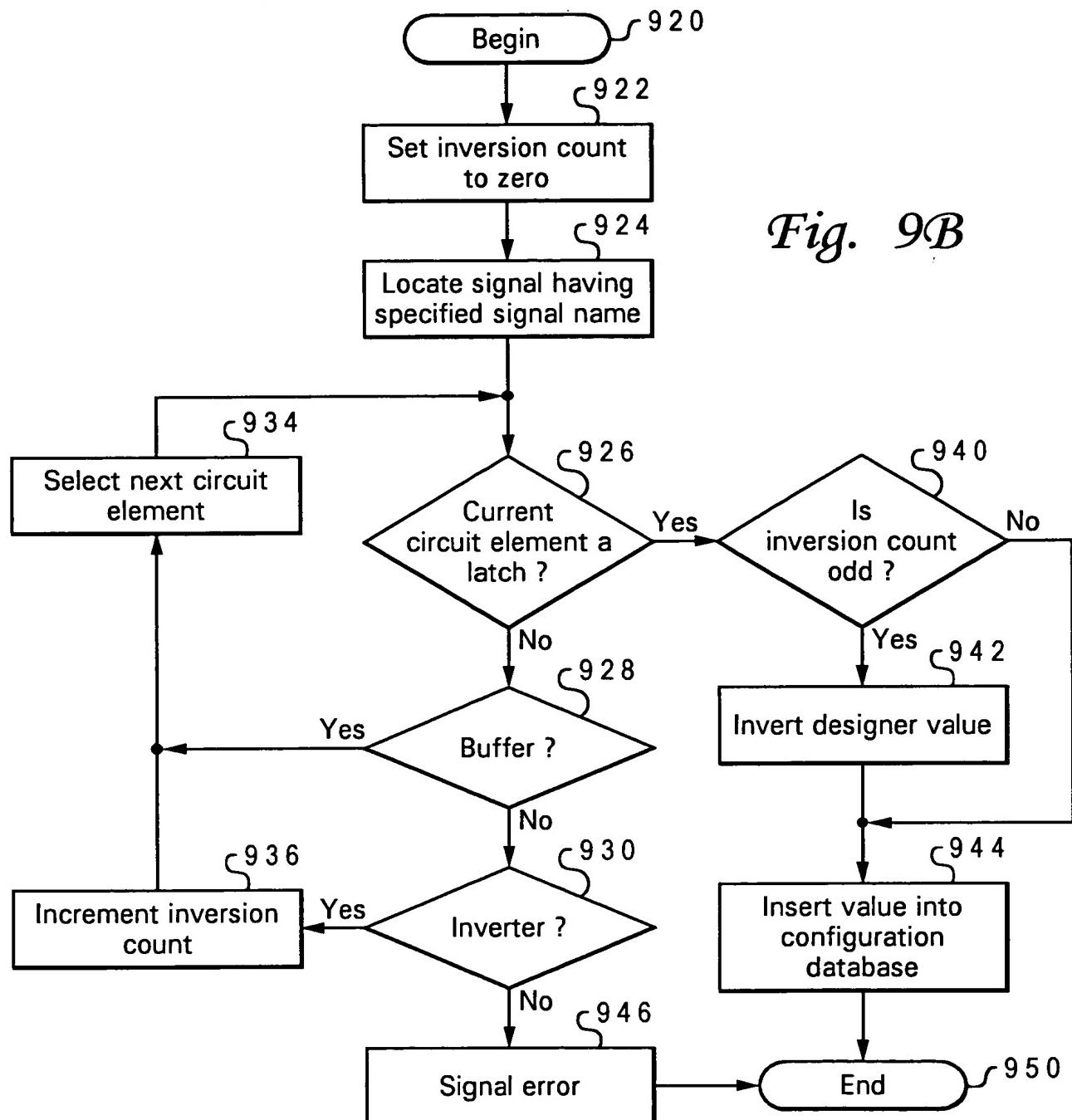
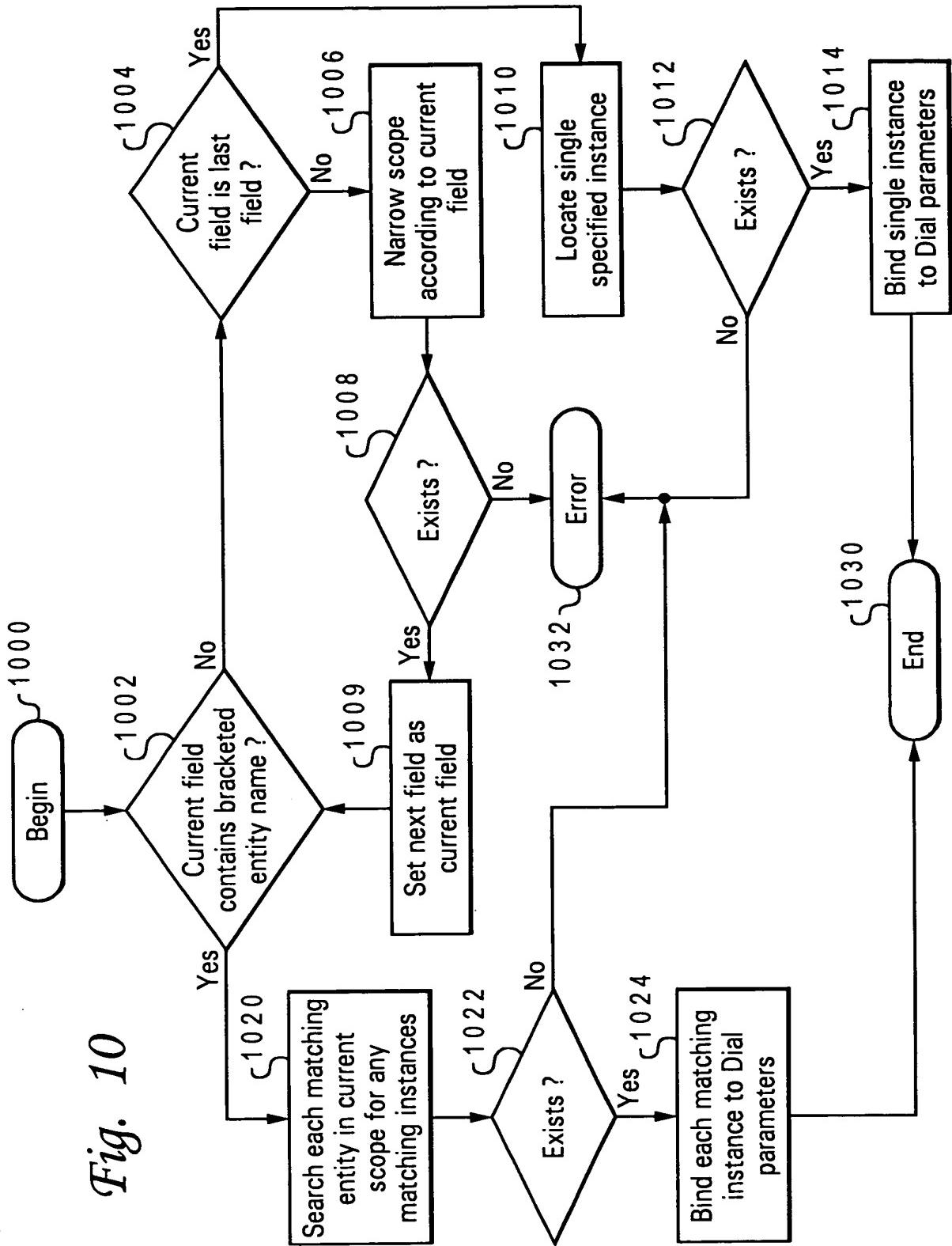


Fig. 10



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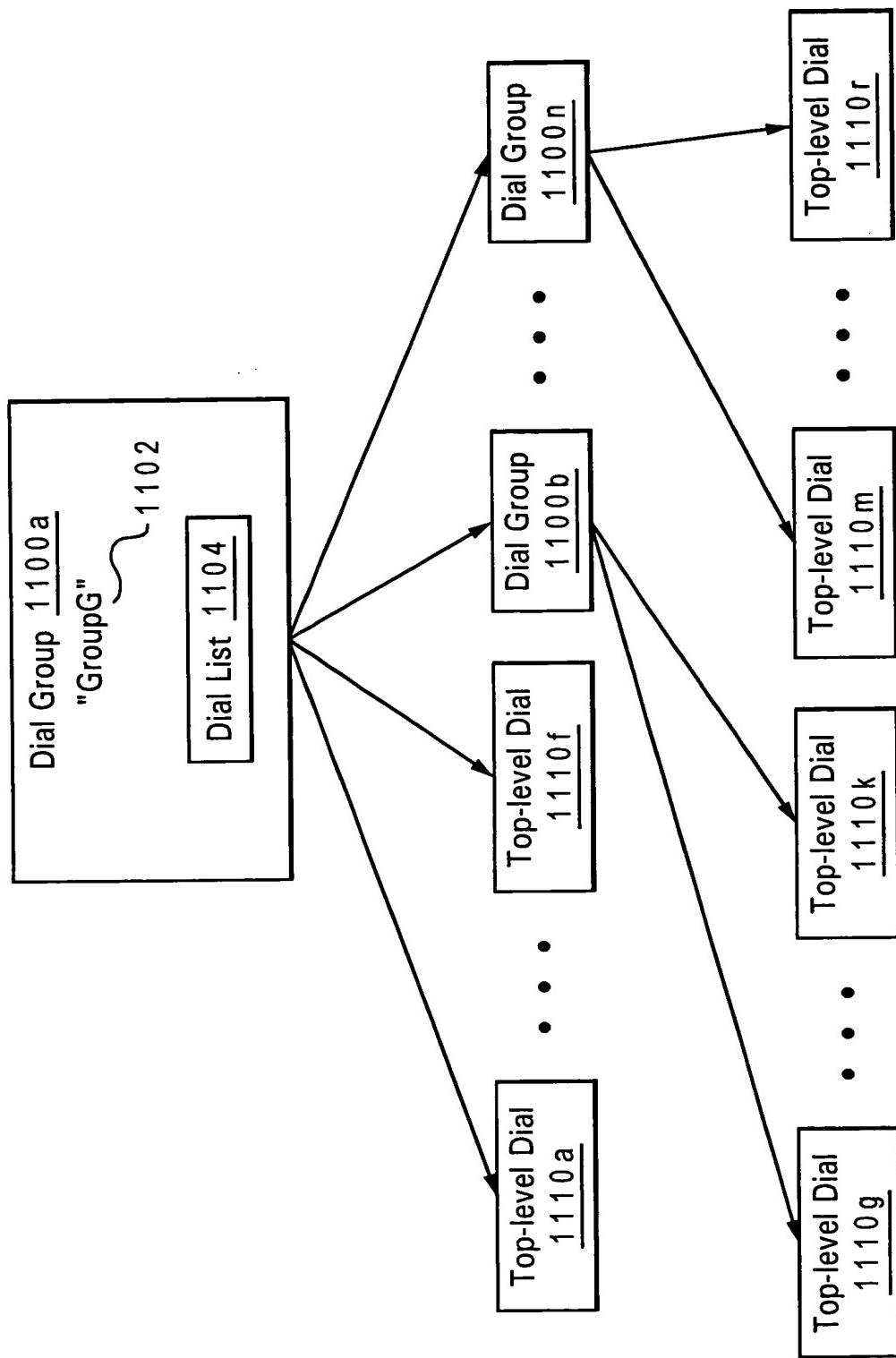


Fig. 11A

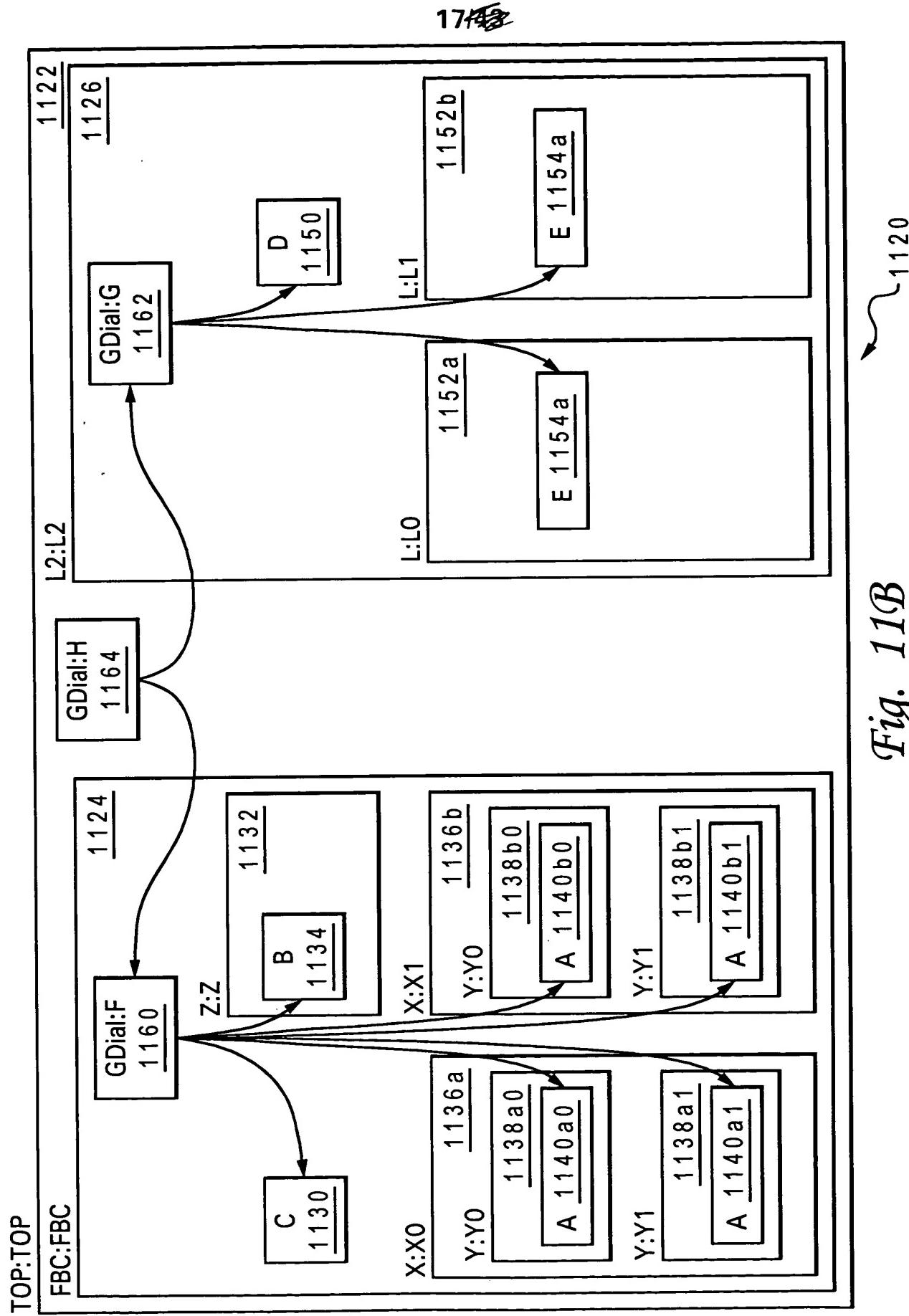


Fig. 11B

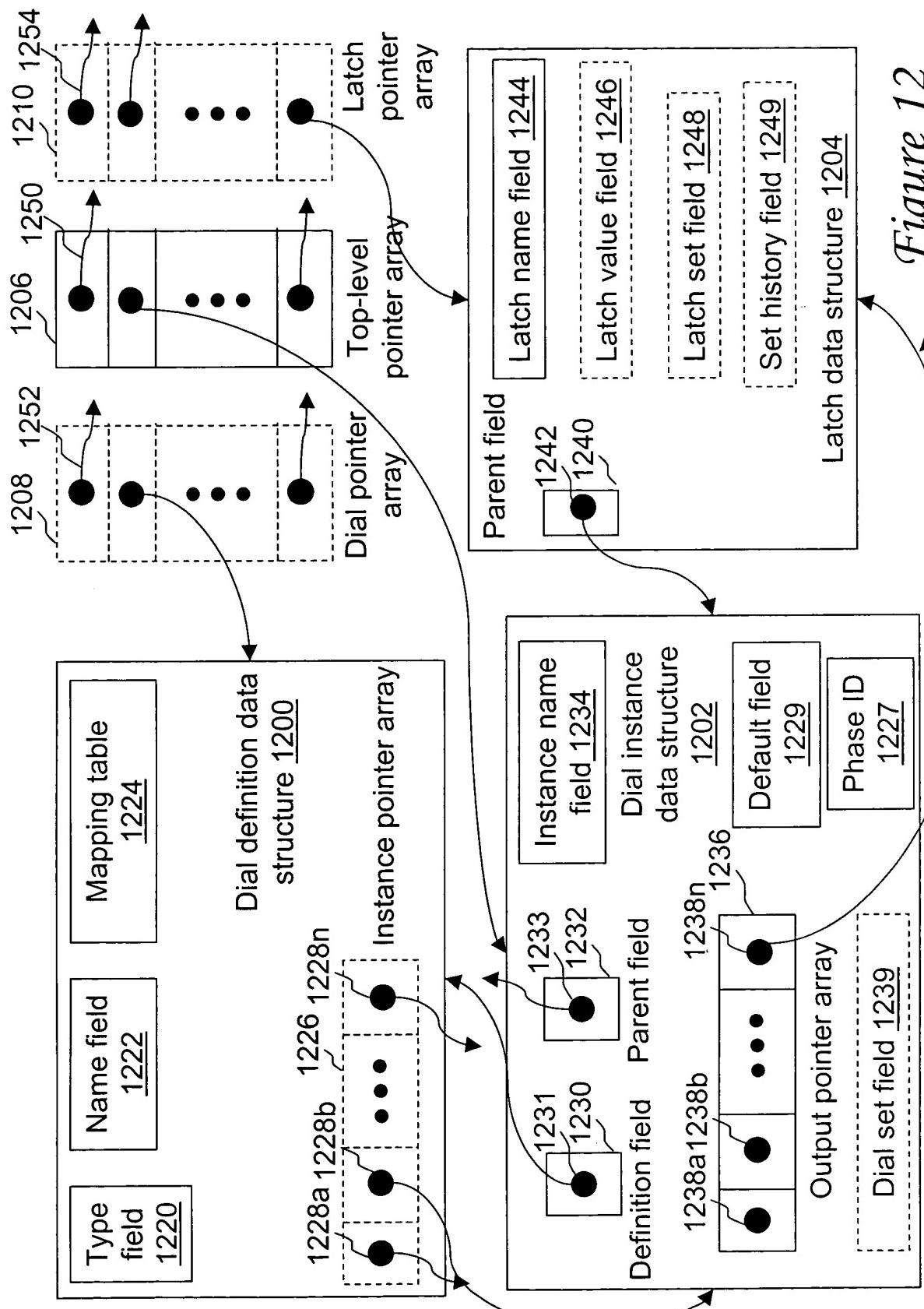


Figure 12

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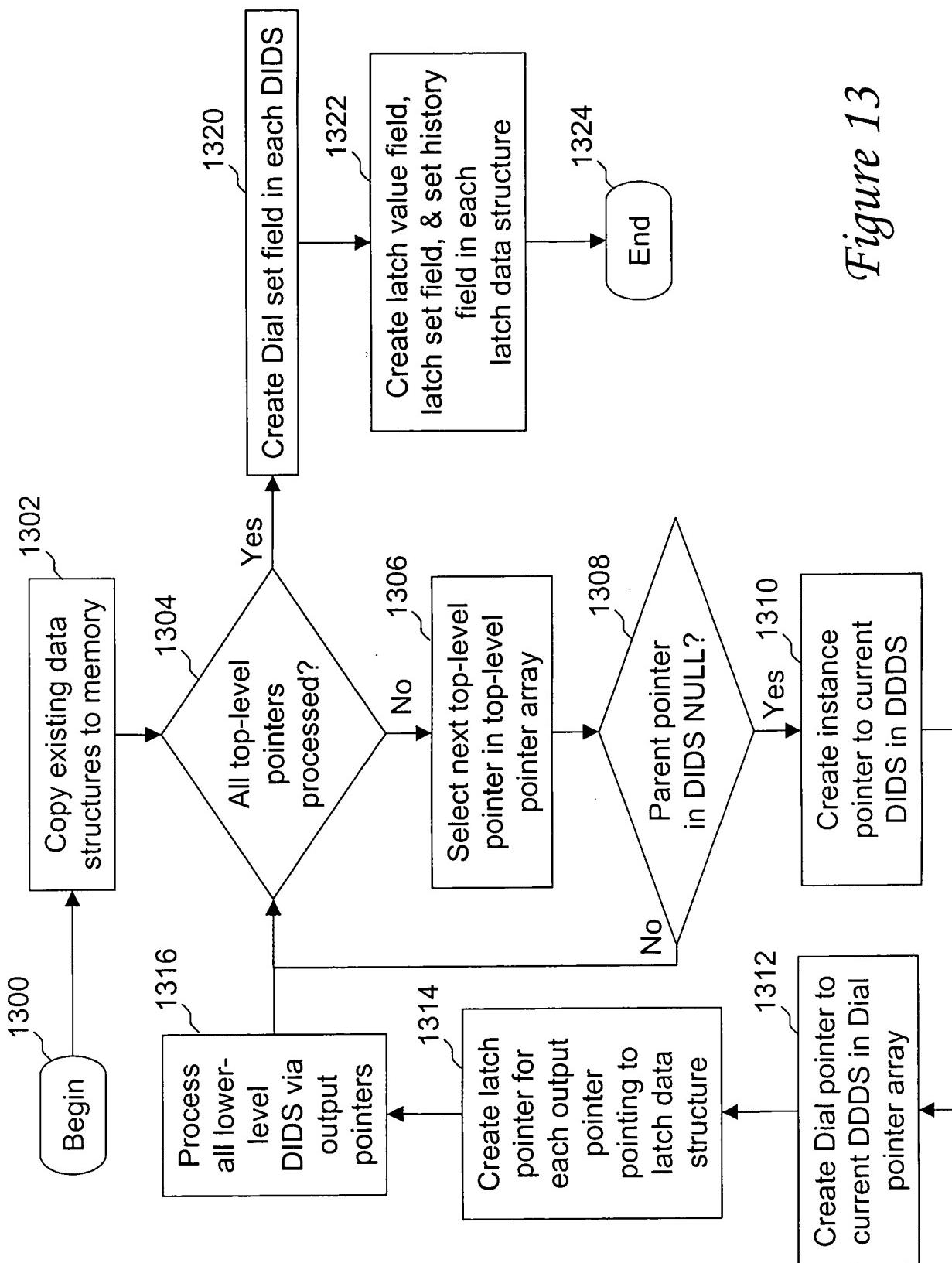
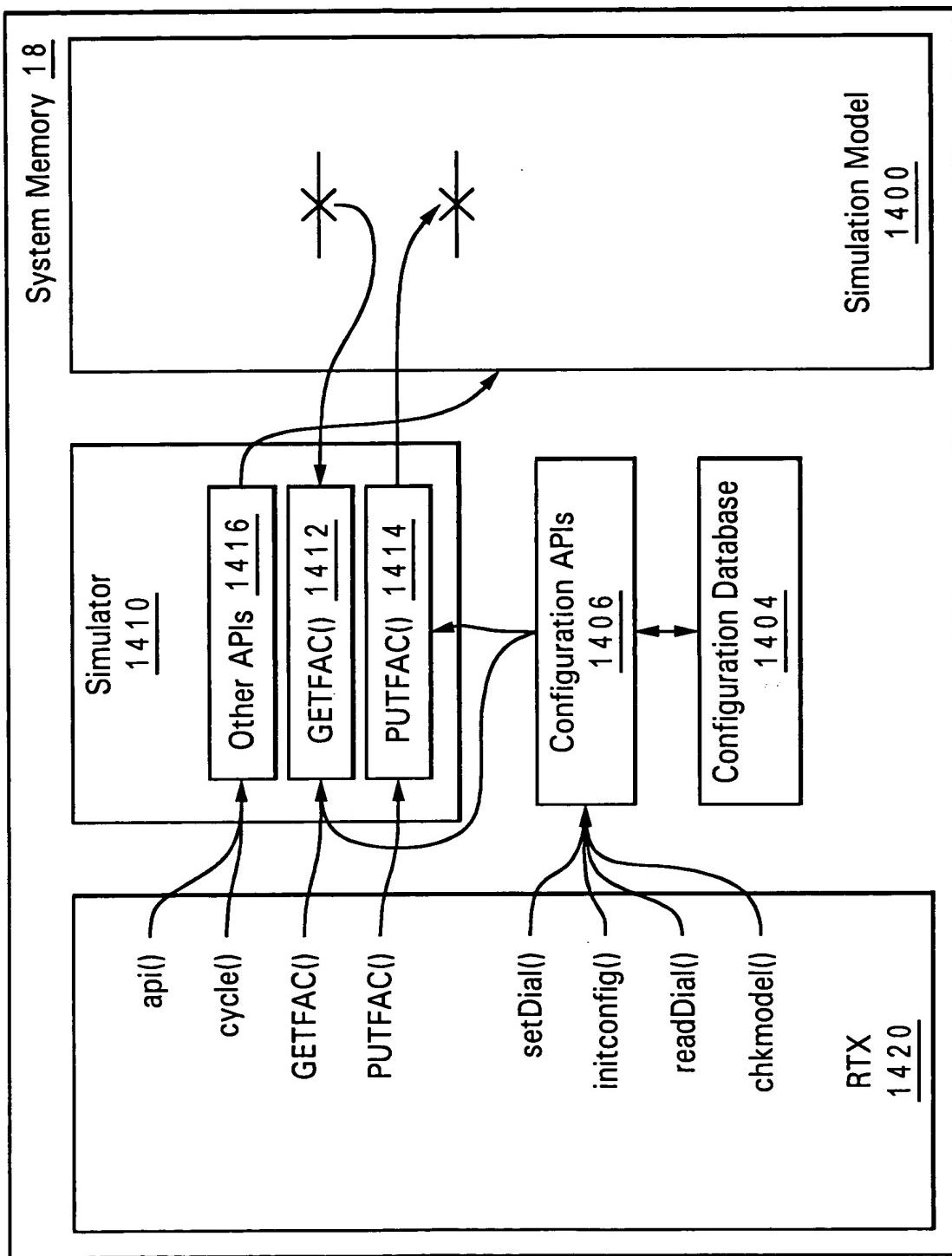


Figure 13

Fig. 14



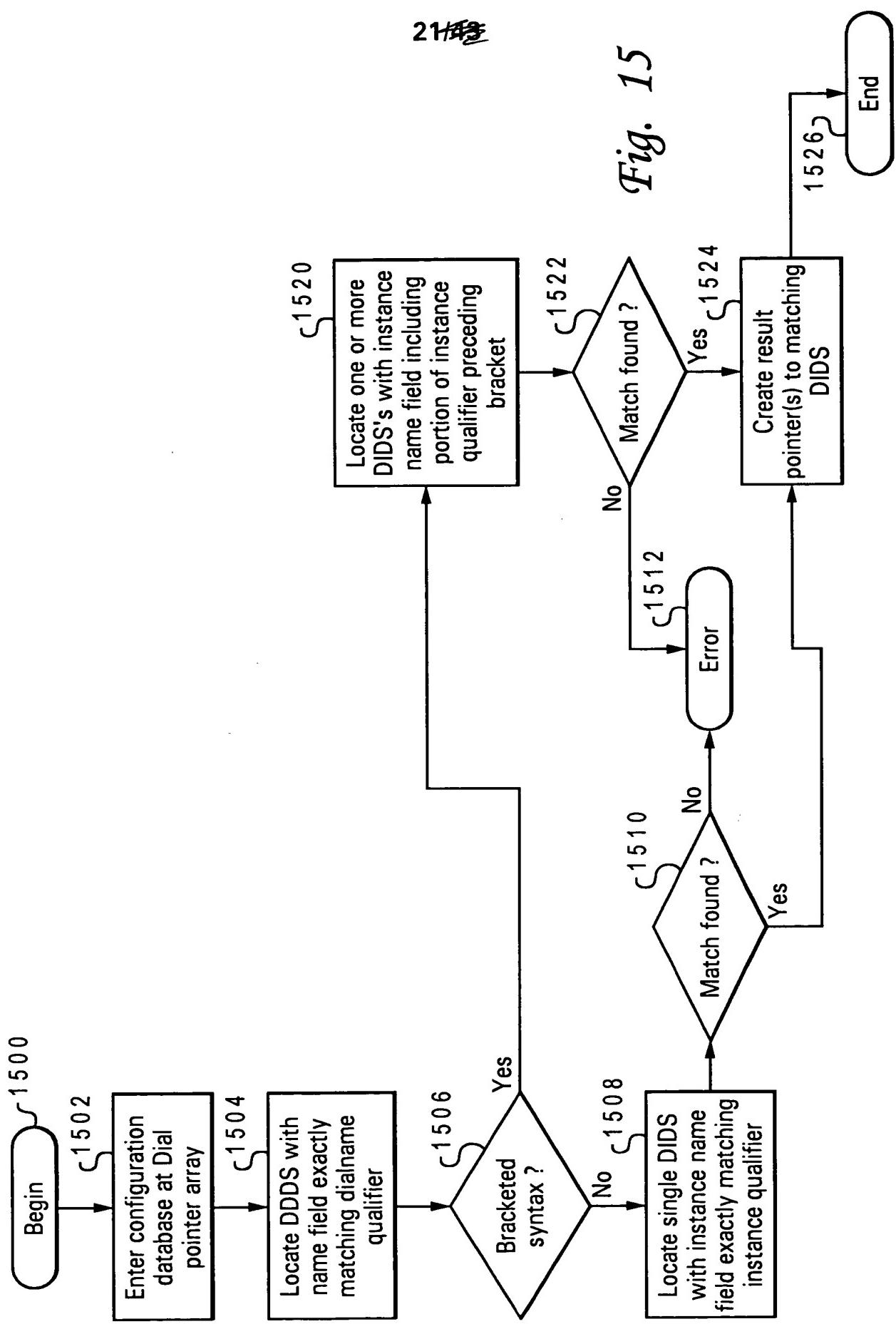


Fig. 16A

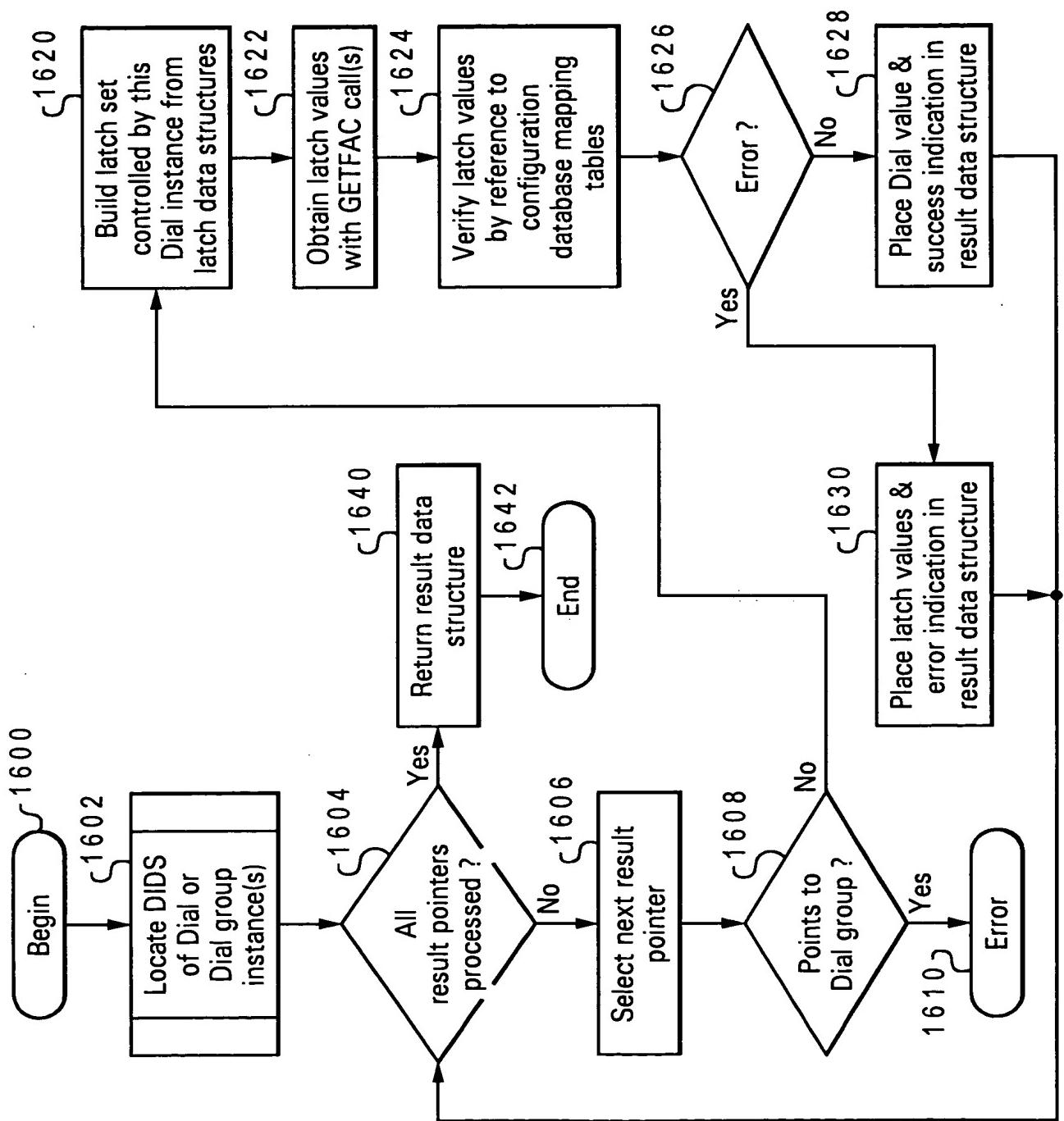


Fig. 16B

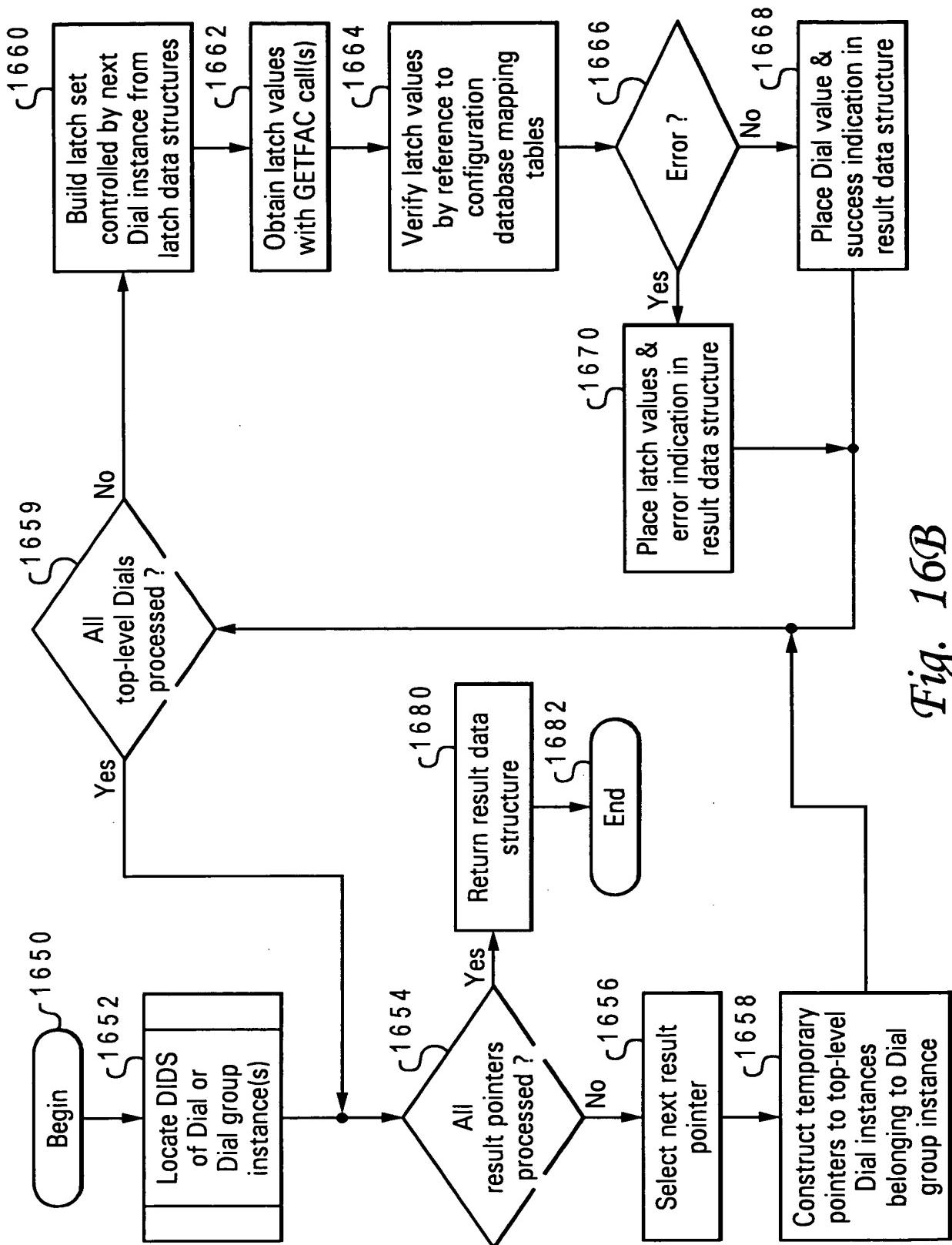
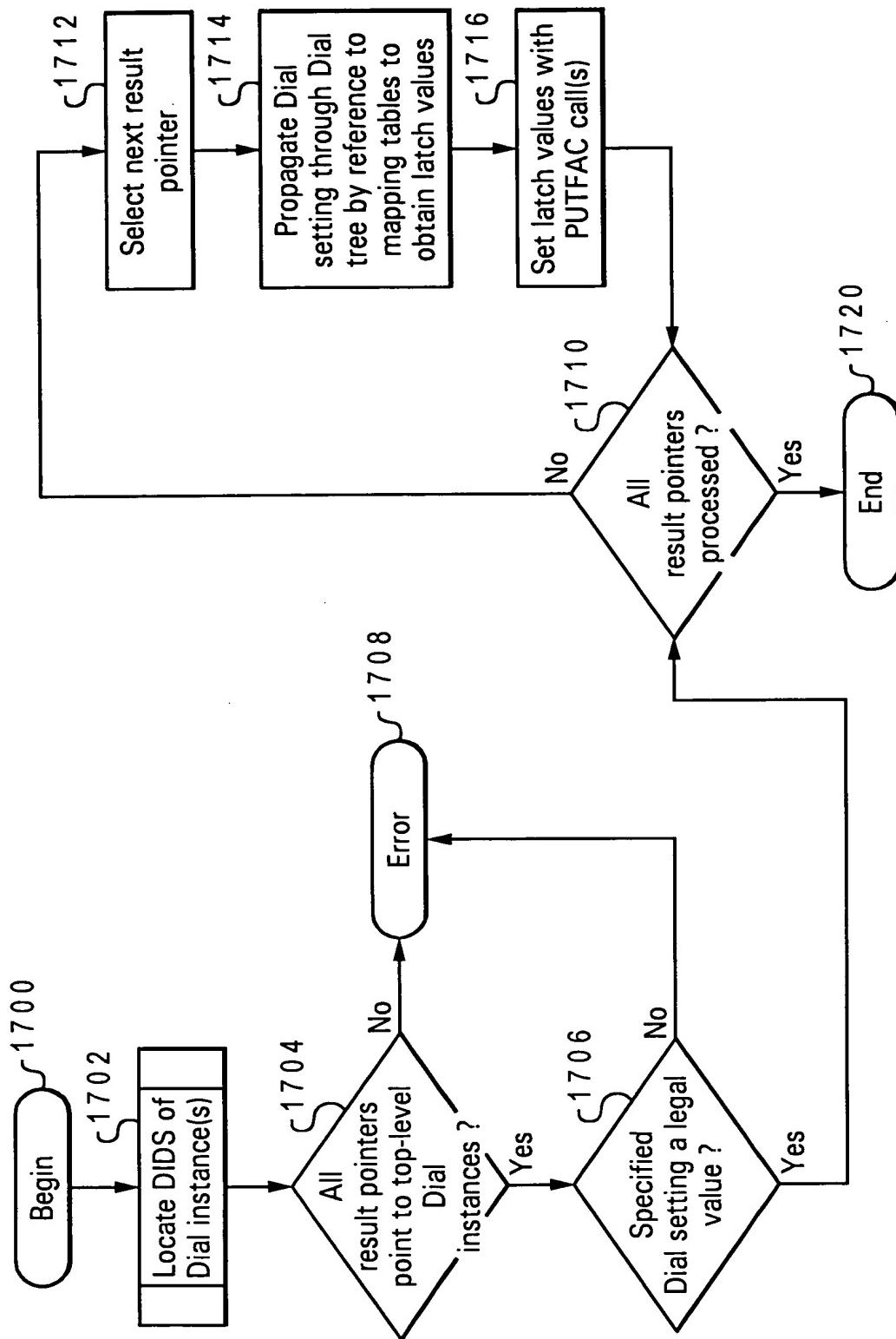


Fig. 17A



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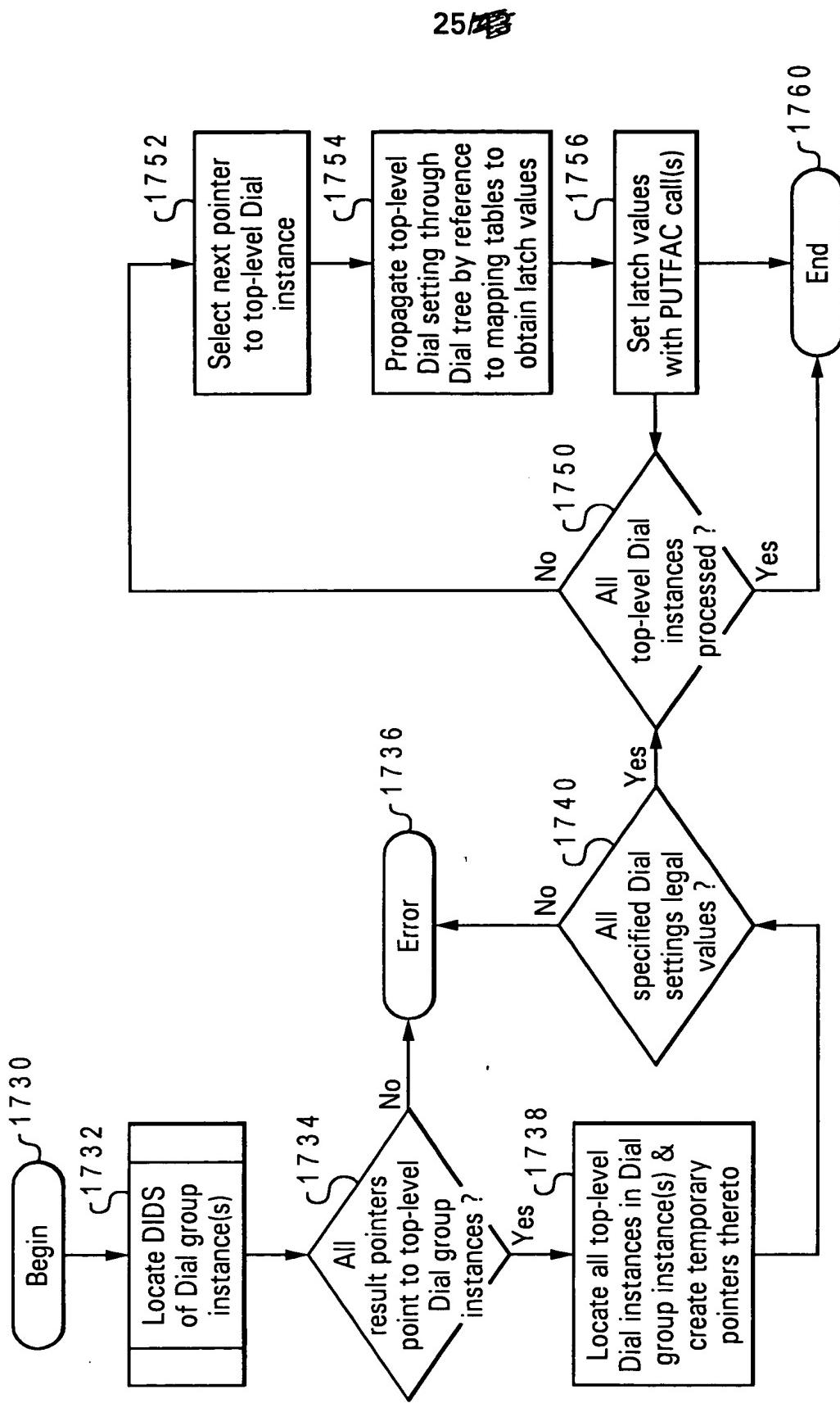


Fig. 17B

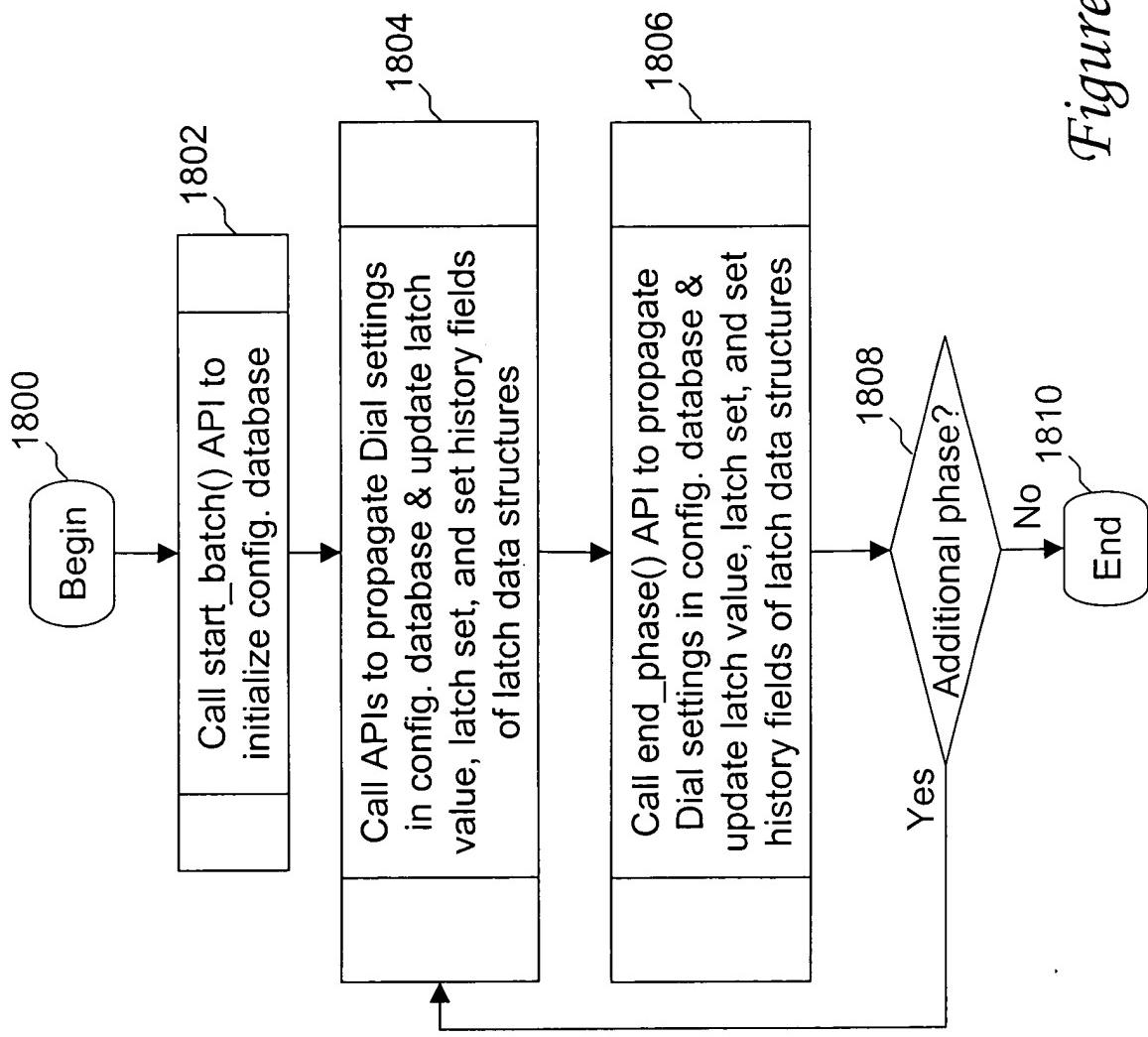


Figure 18A

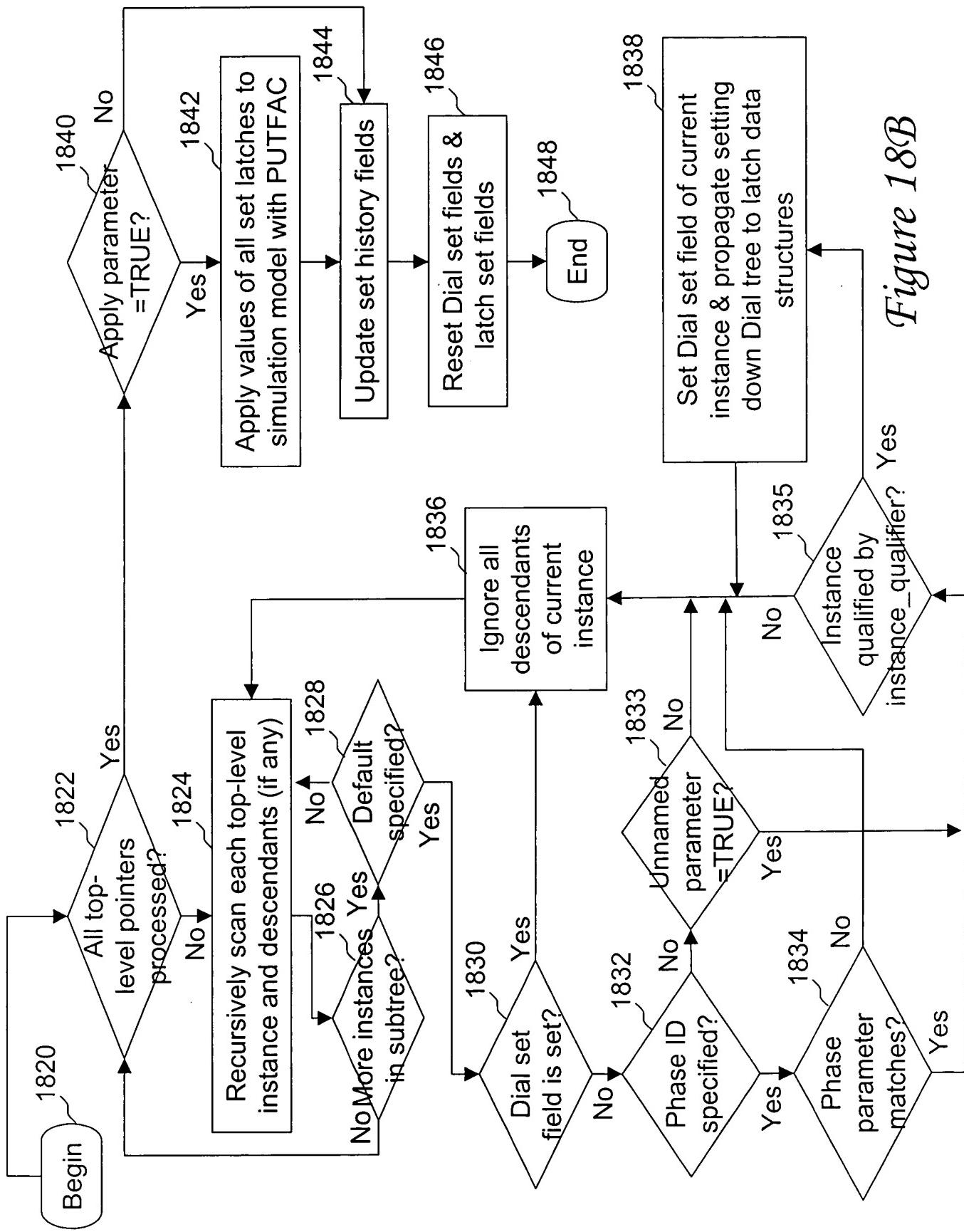


Figure 18B

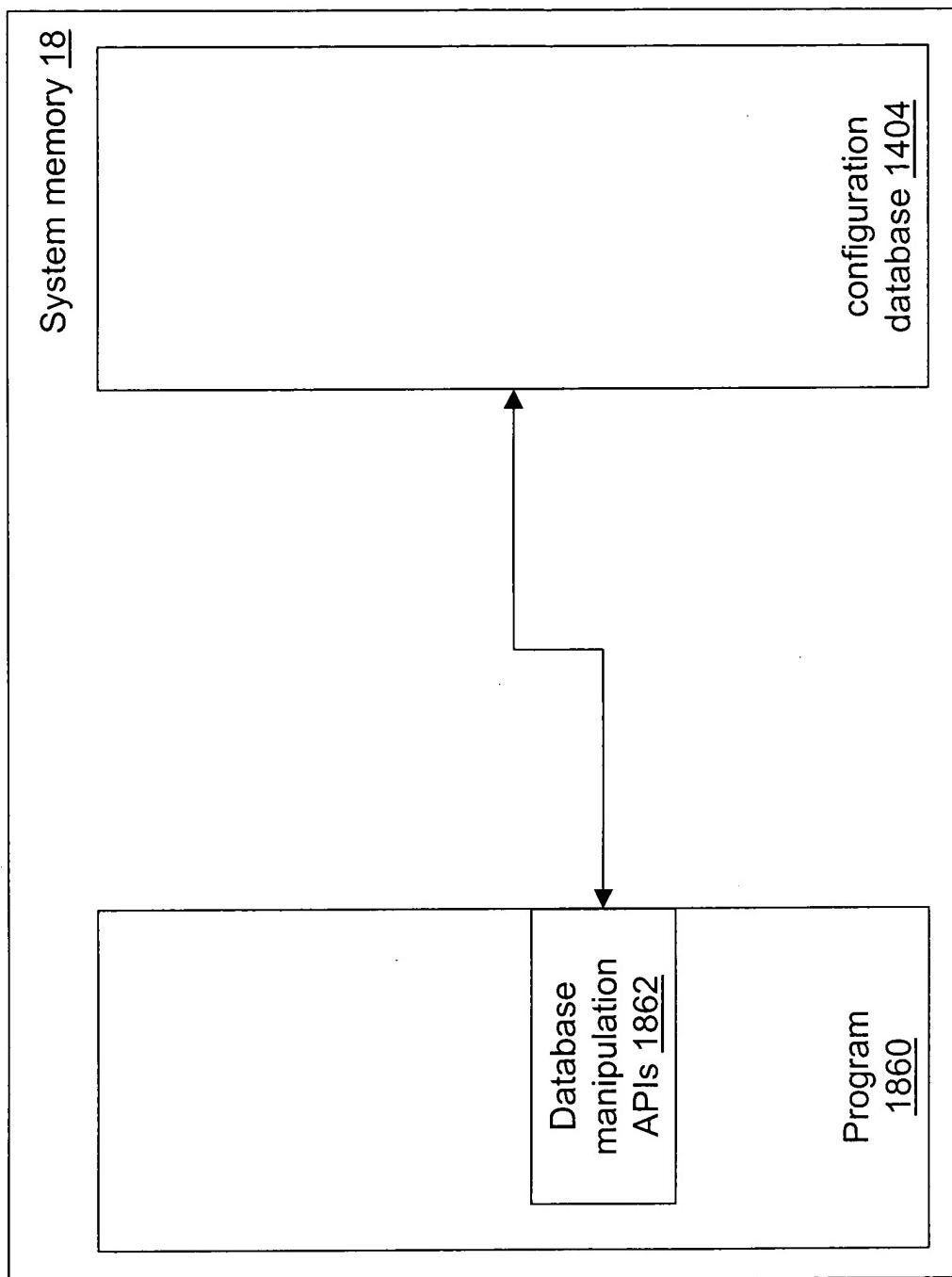


Figure 18C

Fig. 19

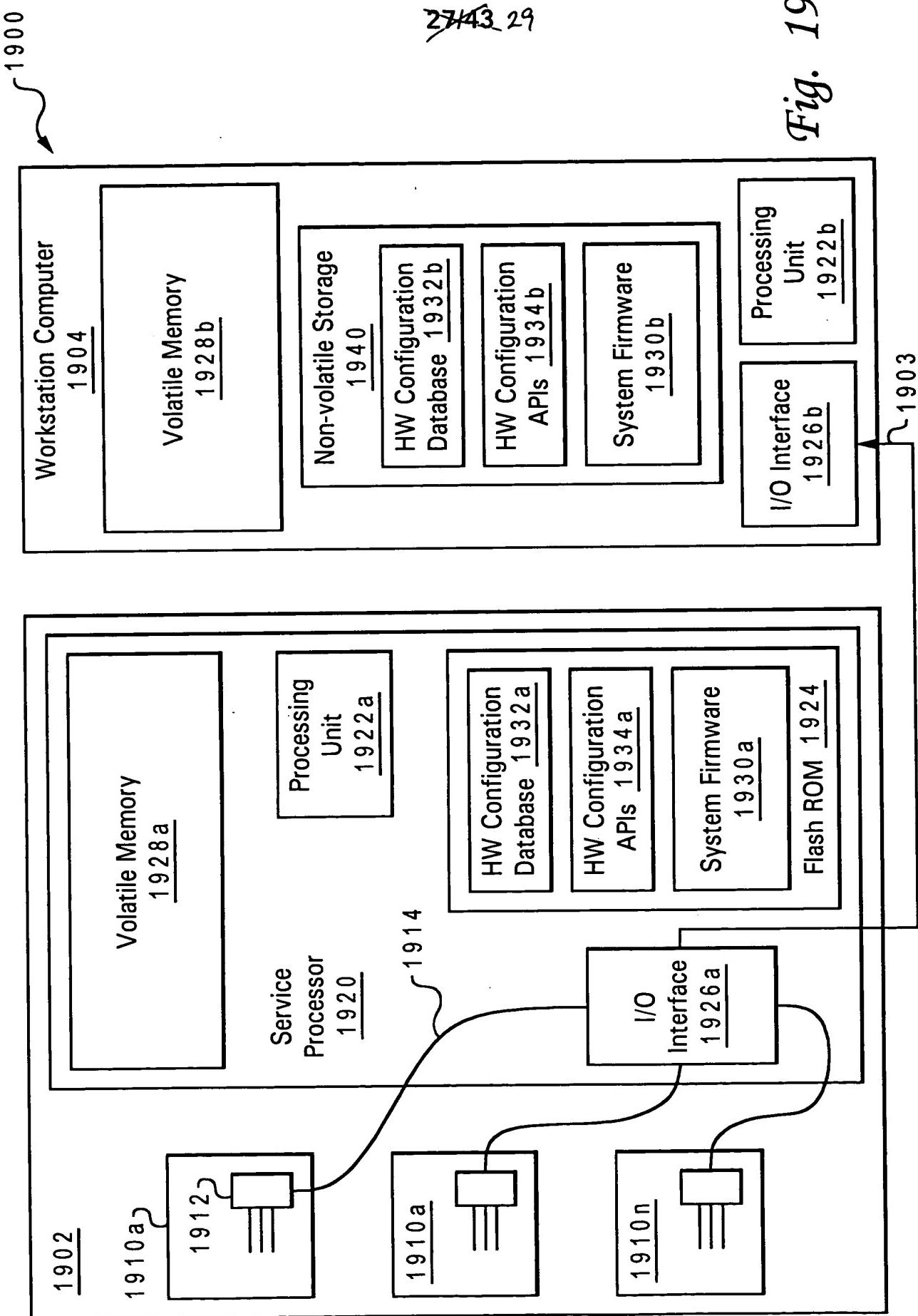
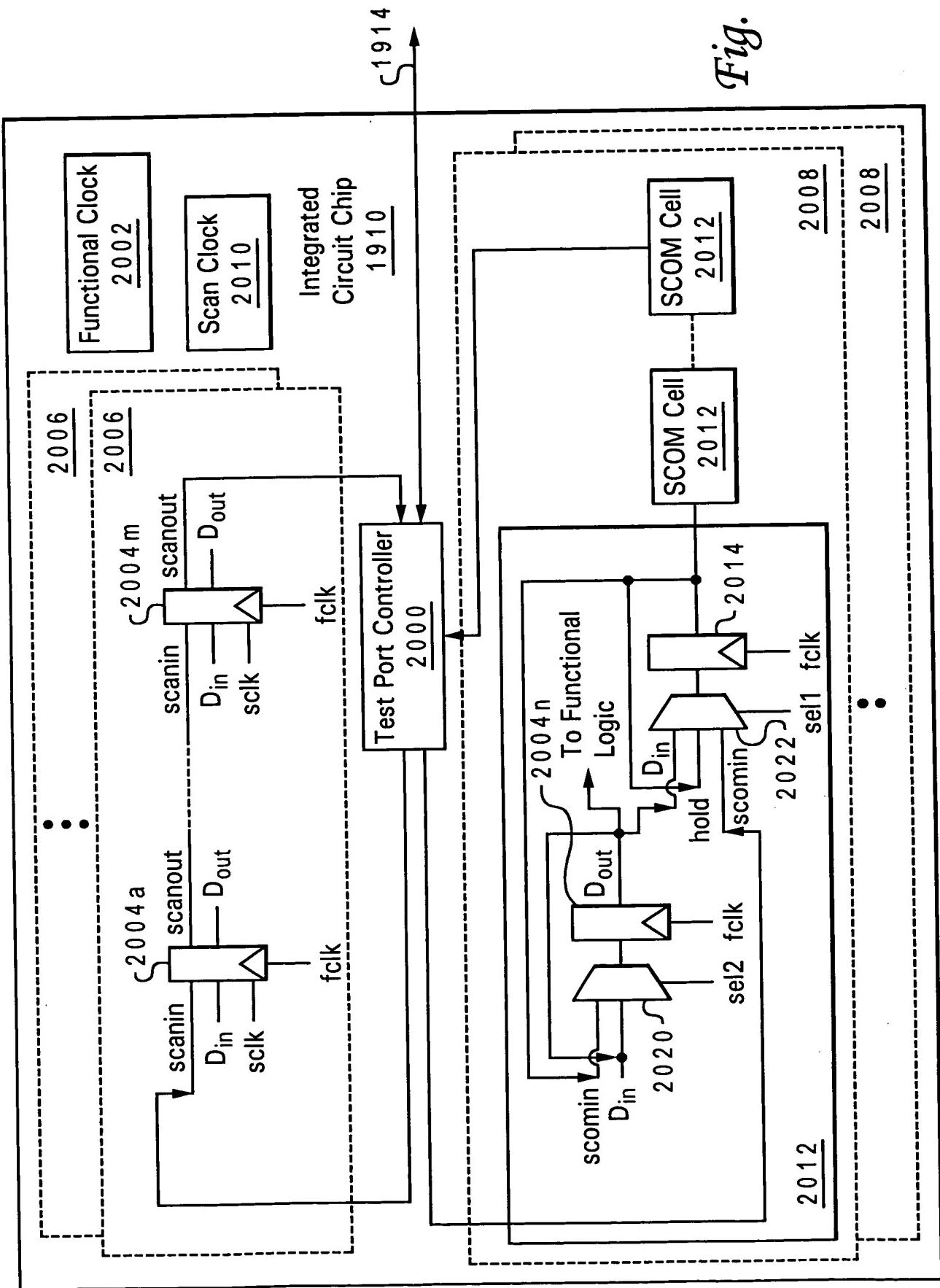


Fig. 20



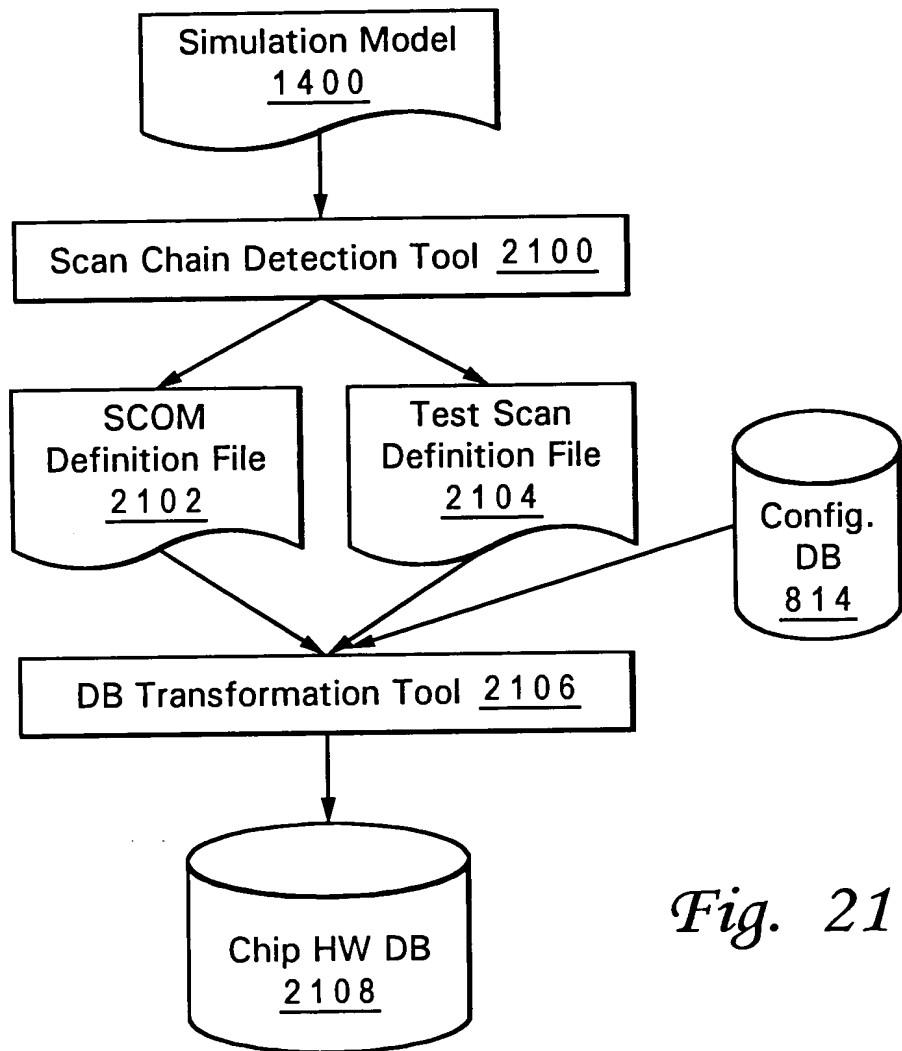
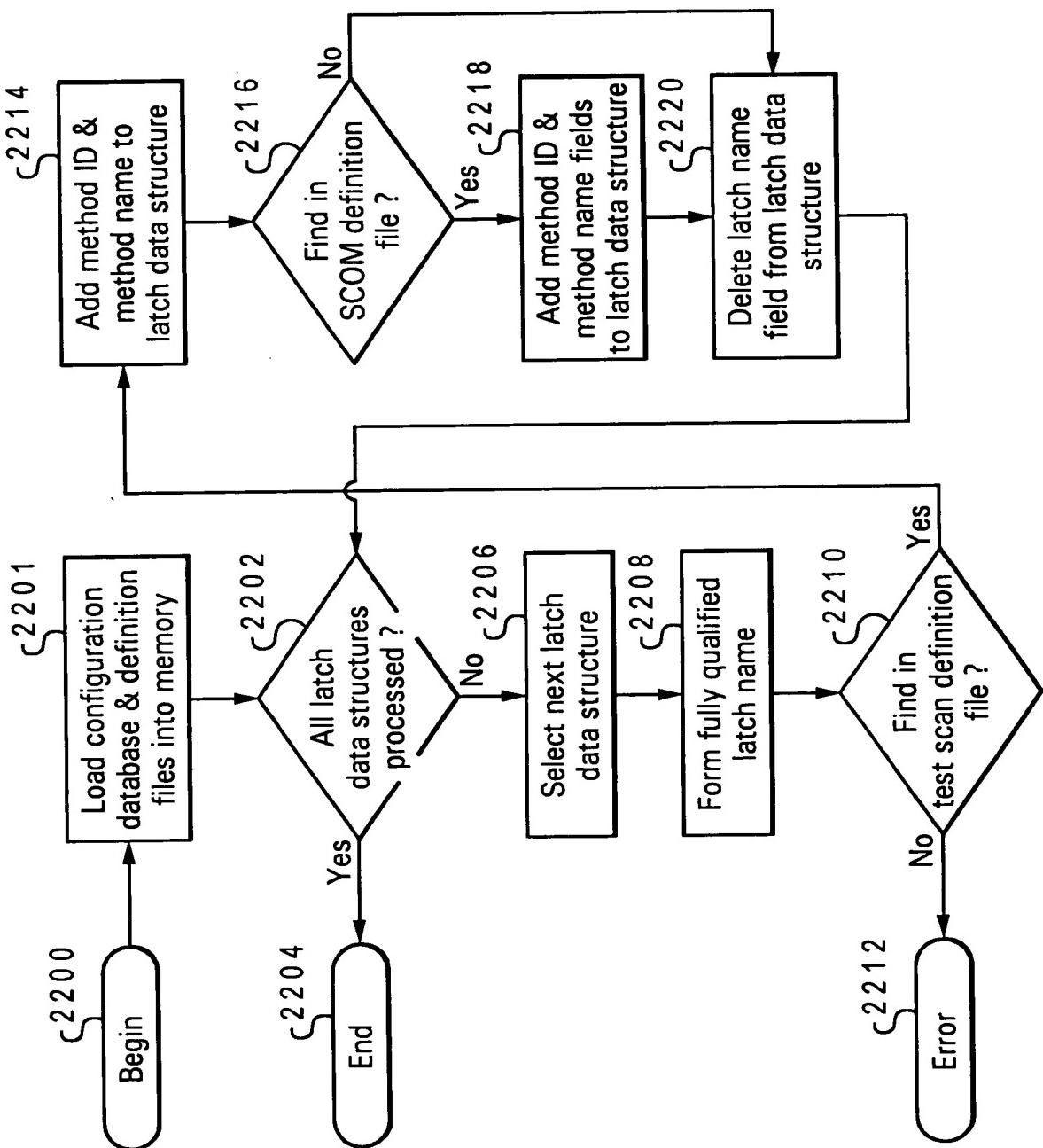


Fig. 21

~~30/43~~ 32
Fig. 22A



~~3143~~ 33

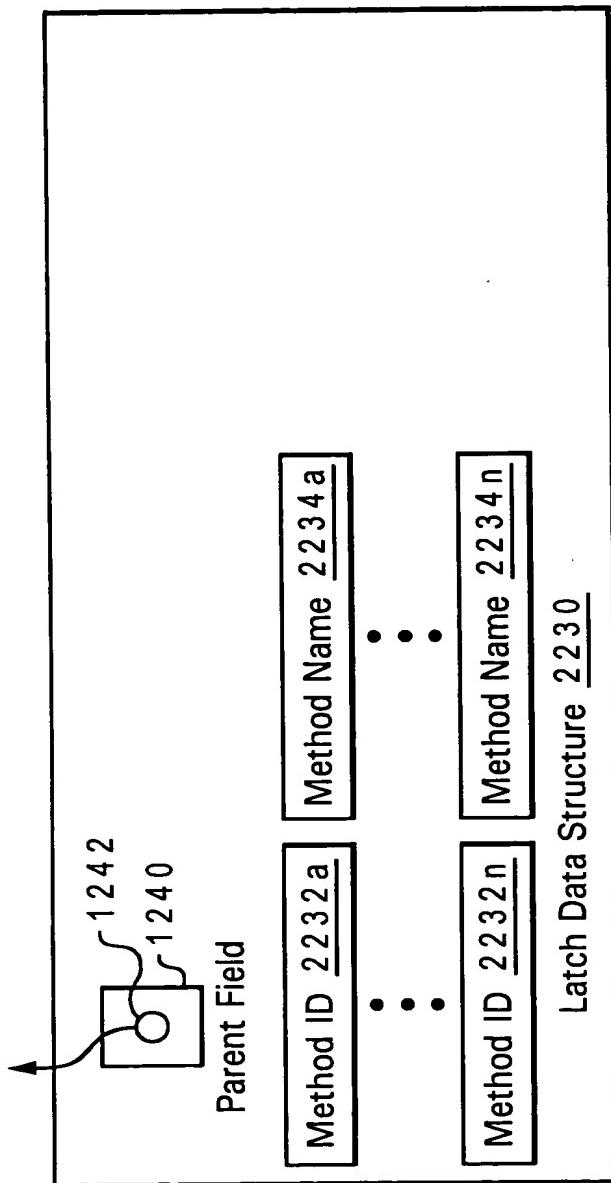


Fig. 22B

~~32/43~~ 34

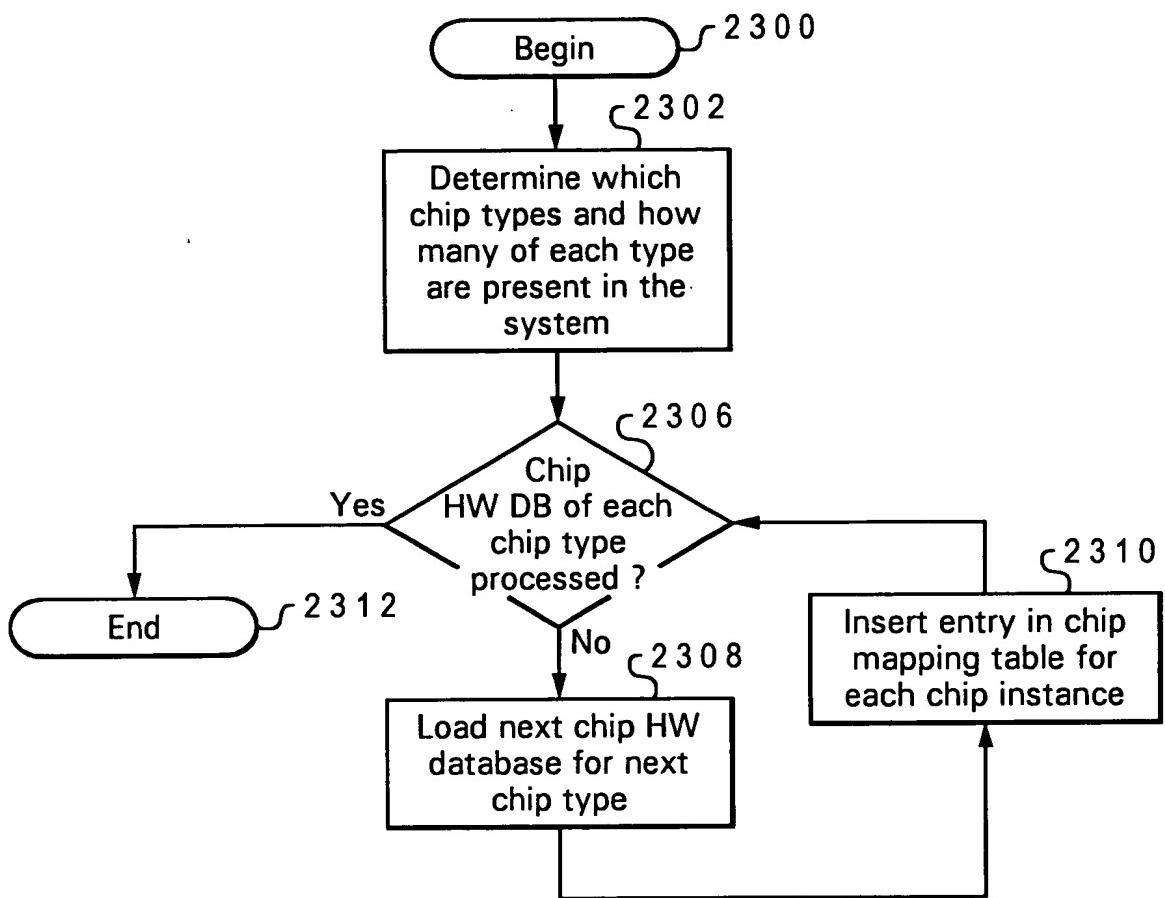


Fig. 23A

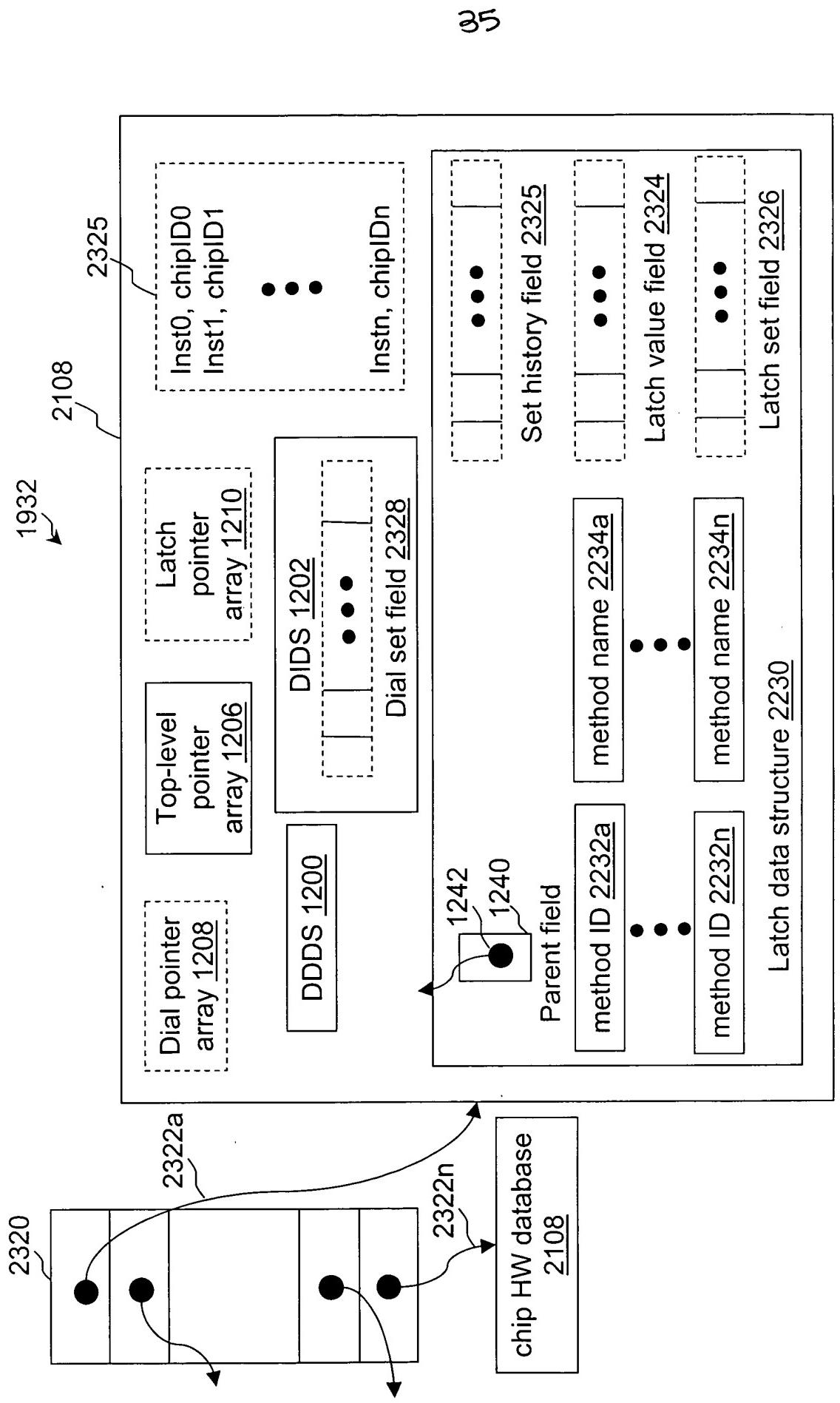
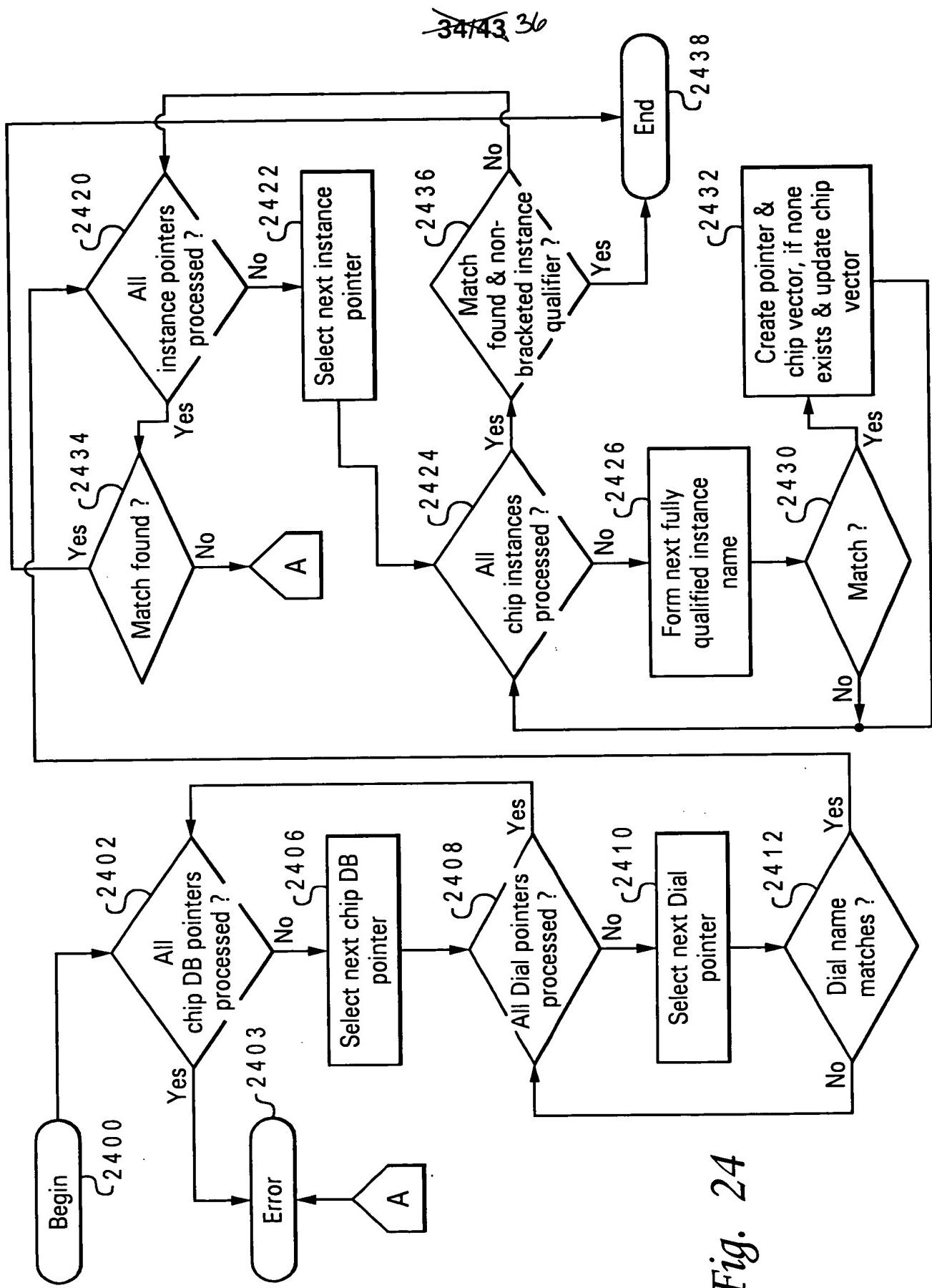


Figure 23B

Fig. 24



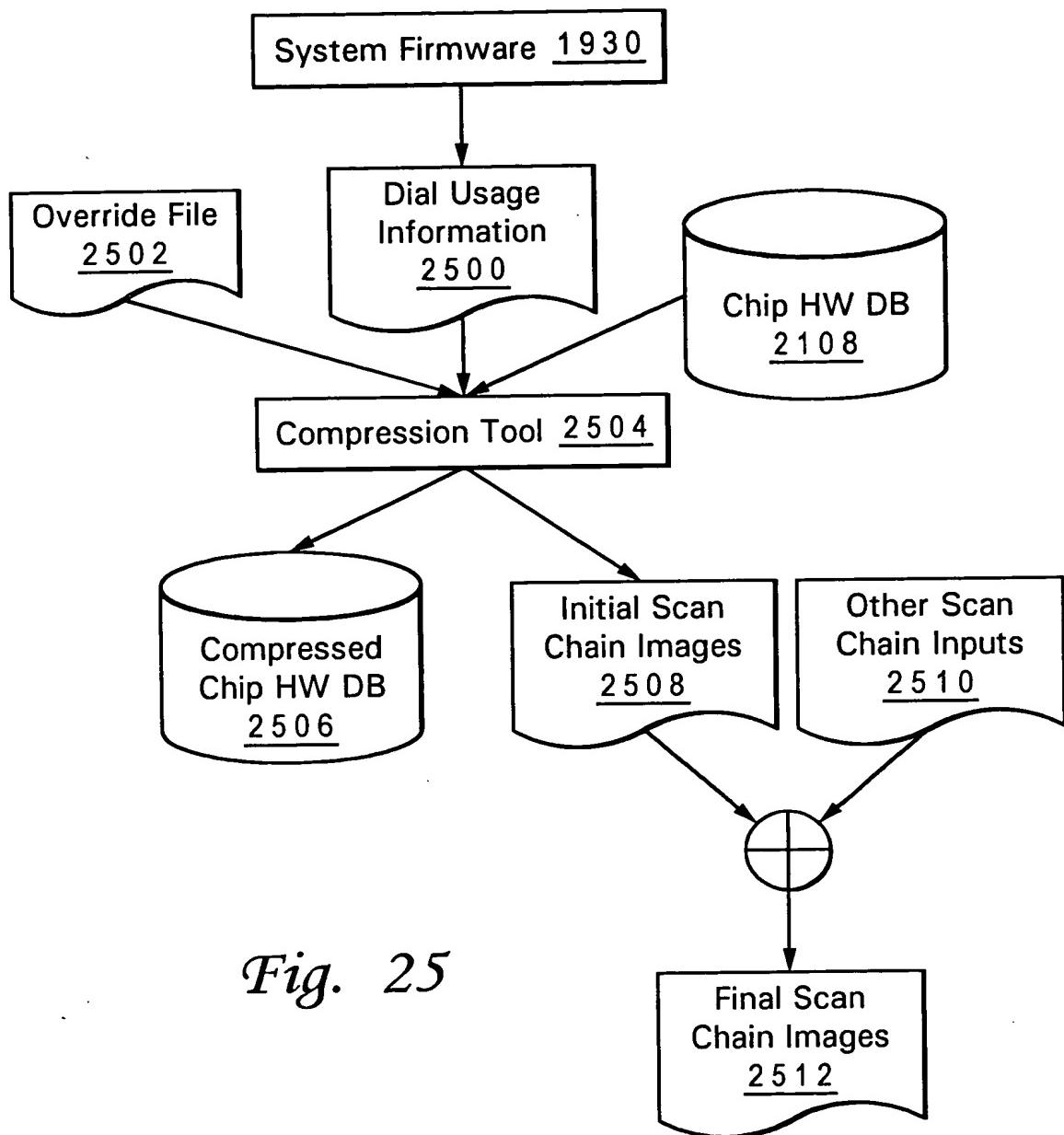
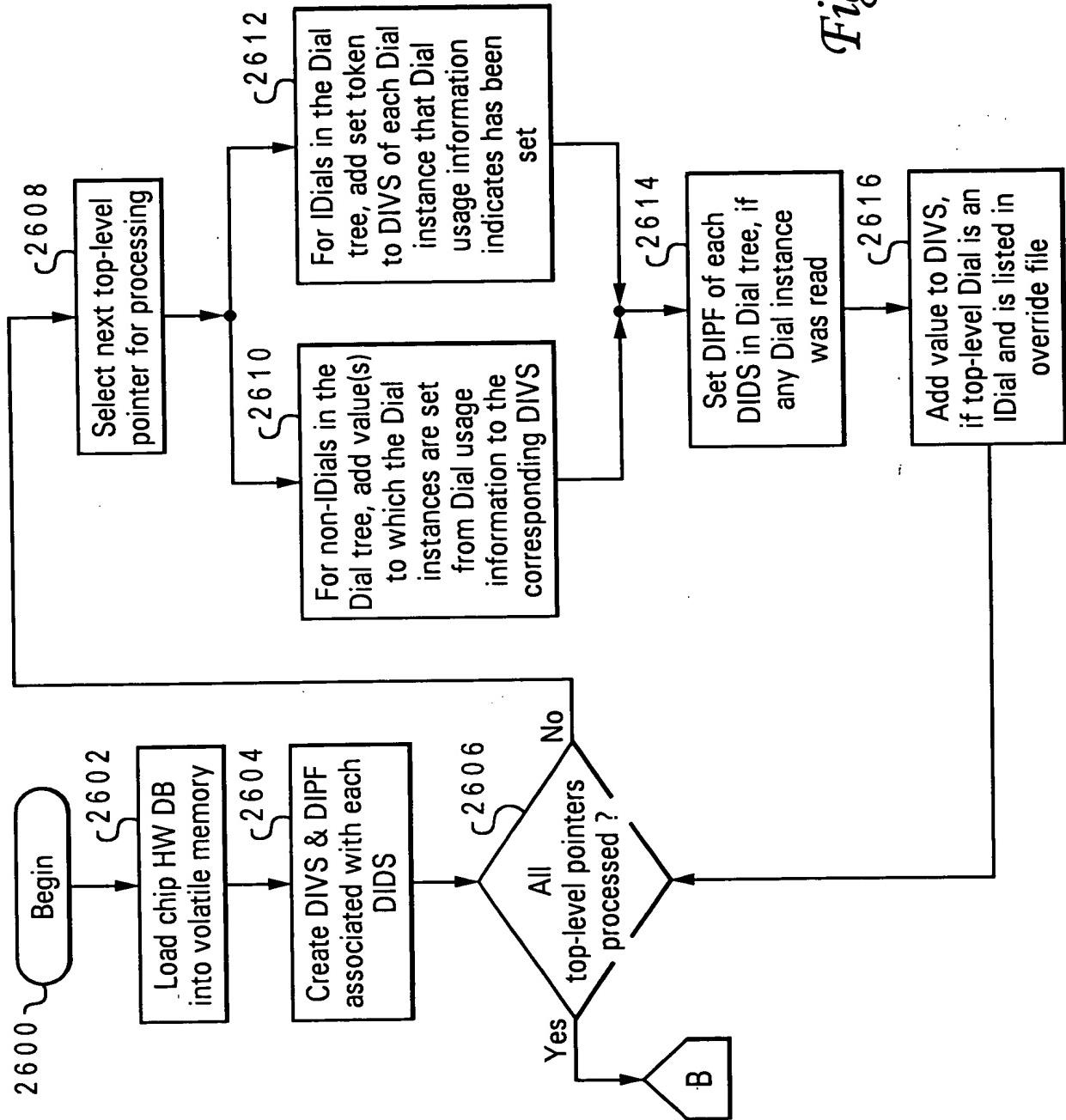


Fig. 25

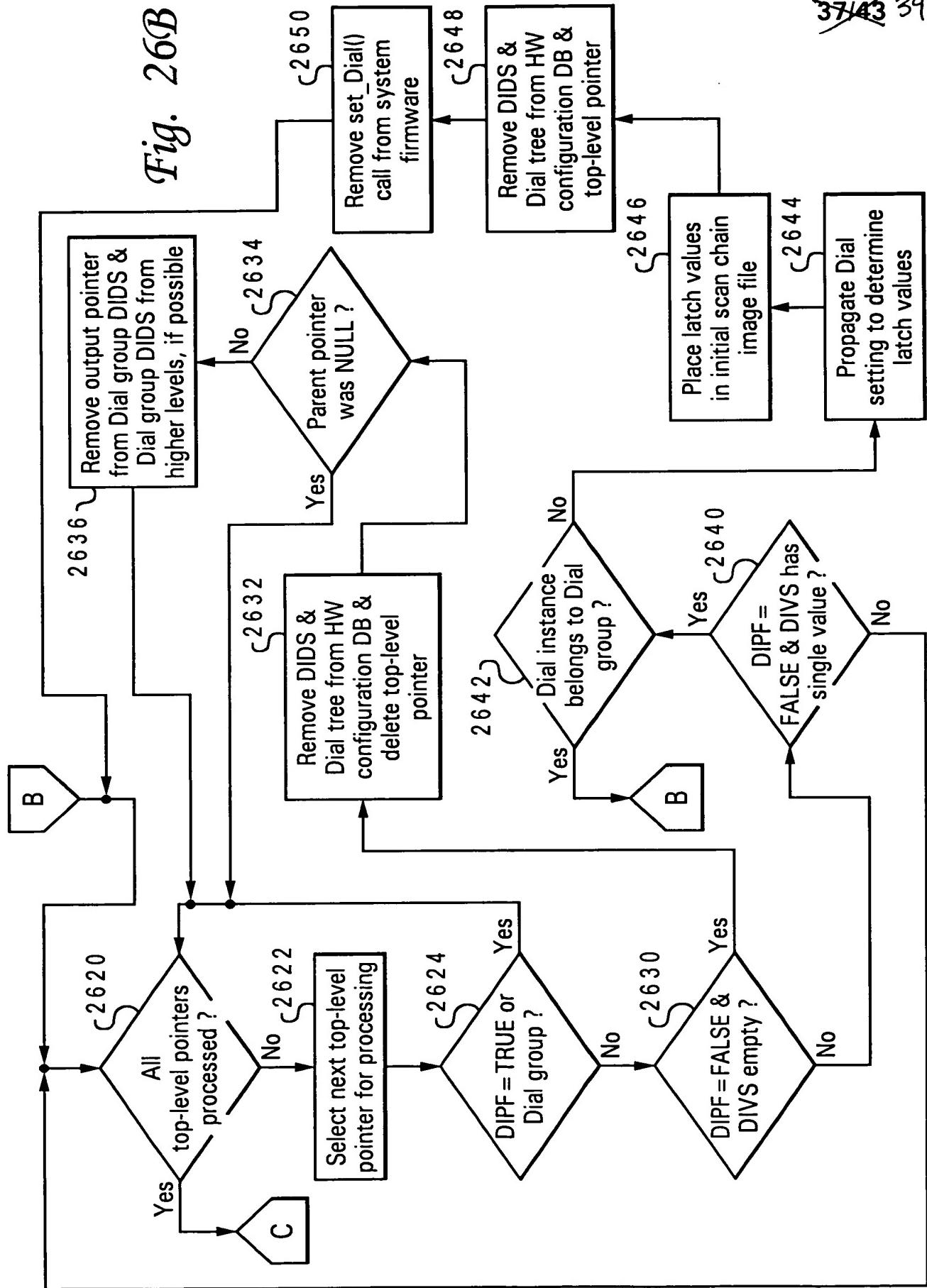
Fig. 26A

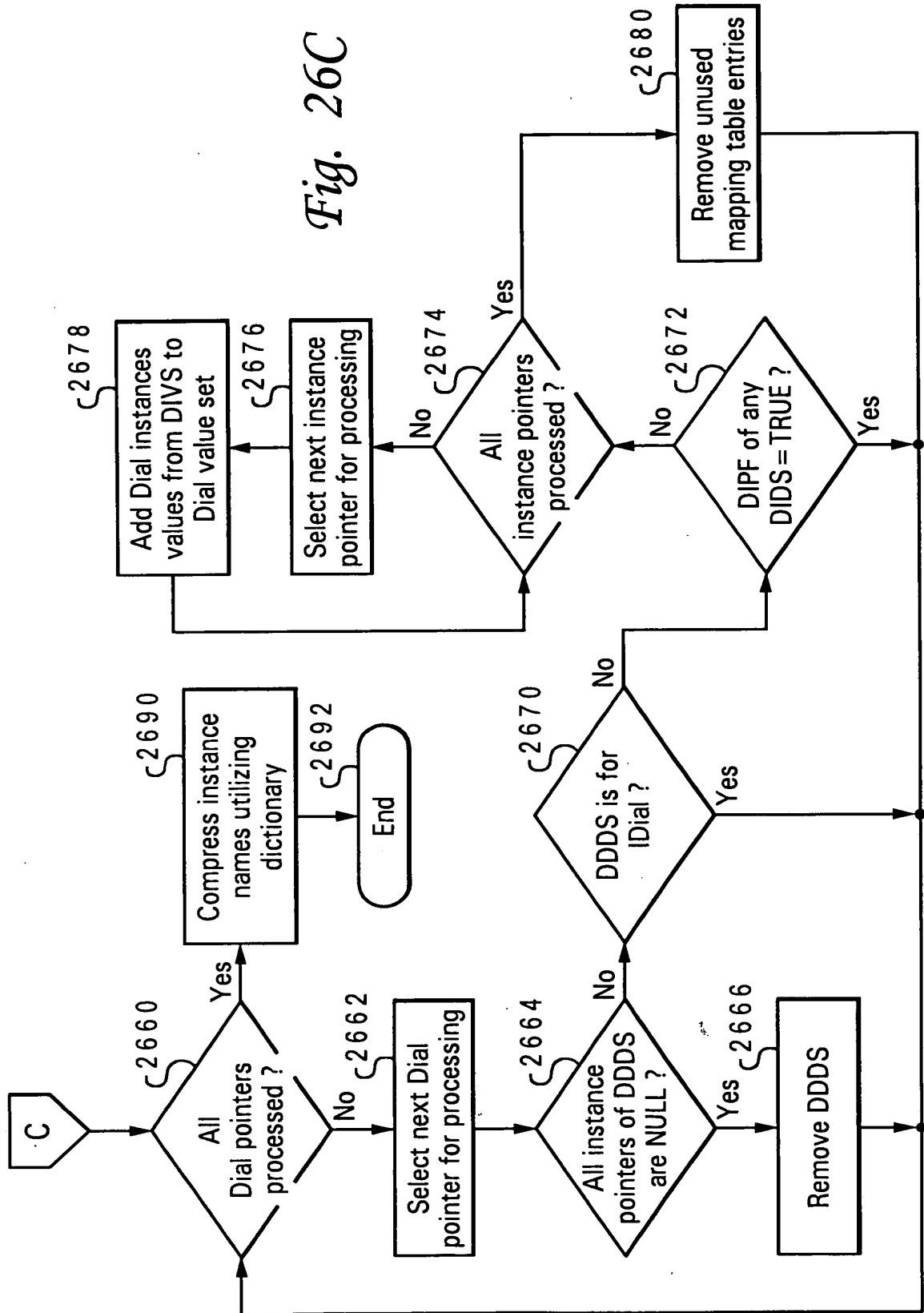


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Fig. 26B

~~37143~~ 39





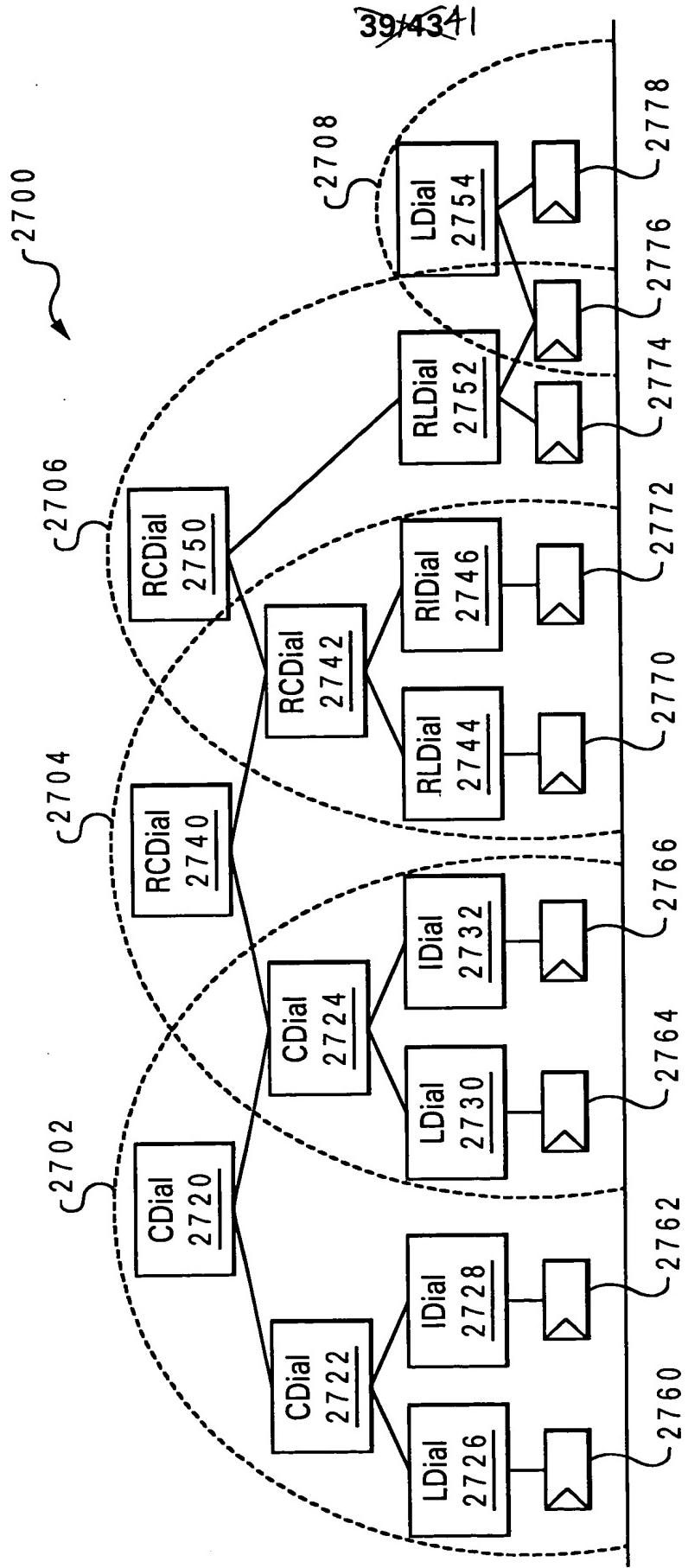


Fig. 27

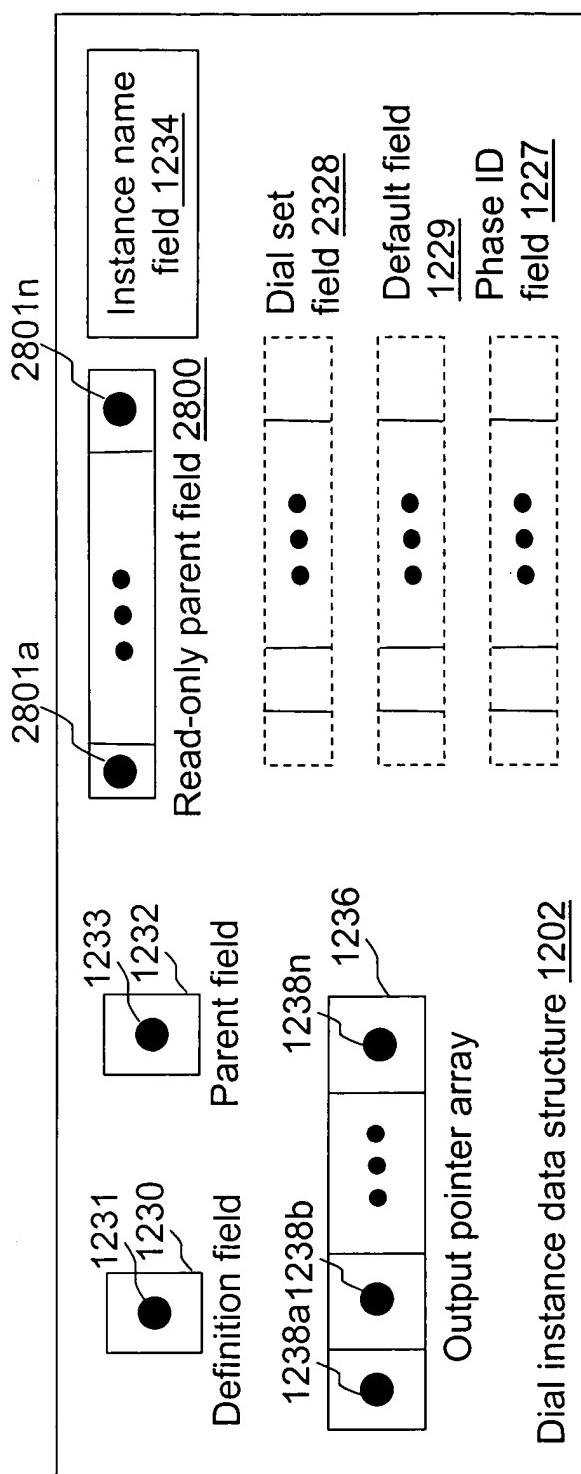


Figure 28A

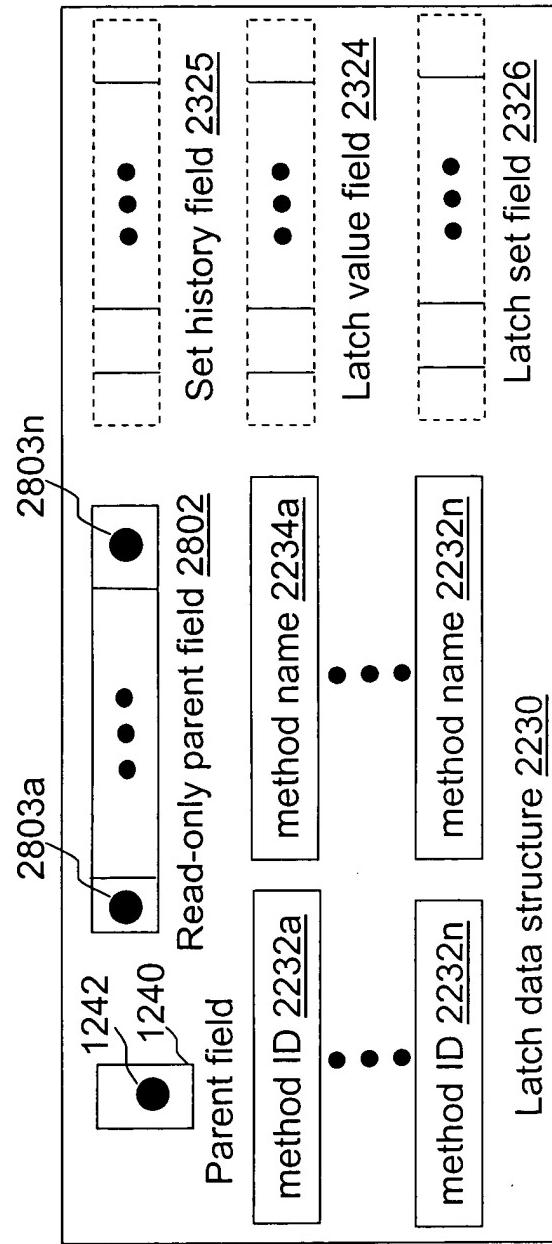
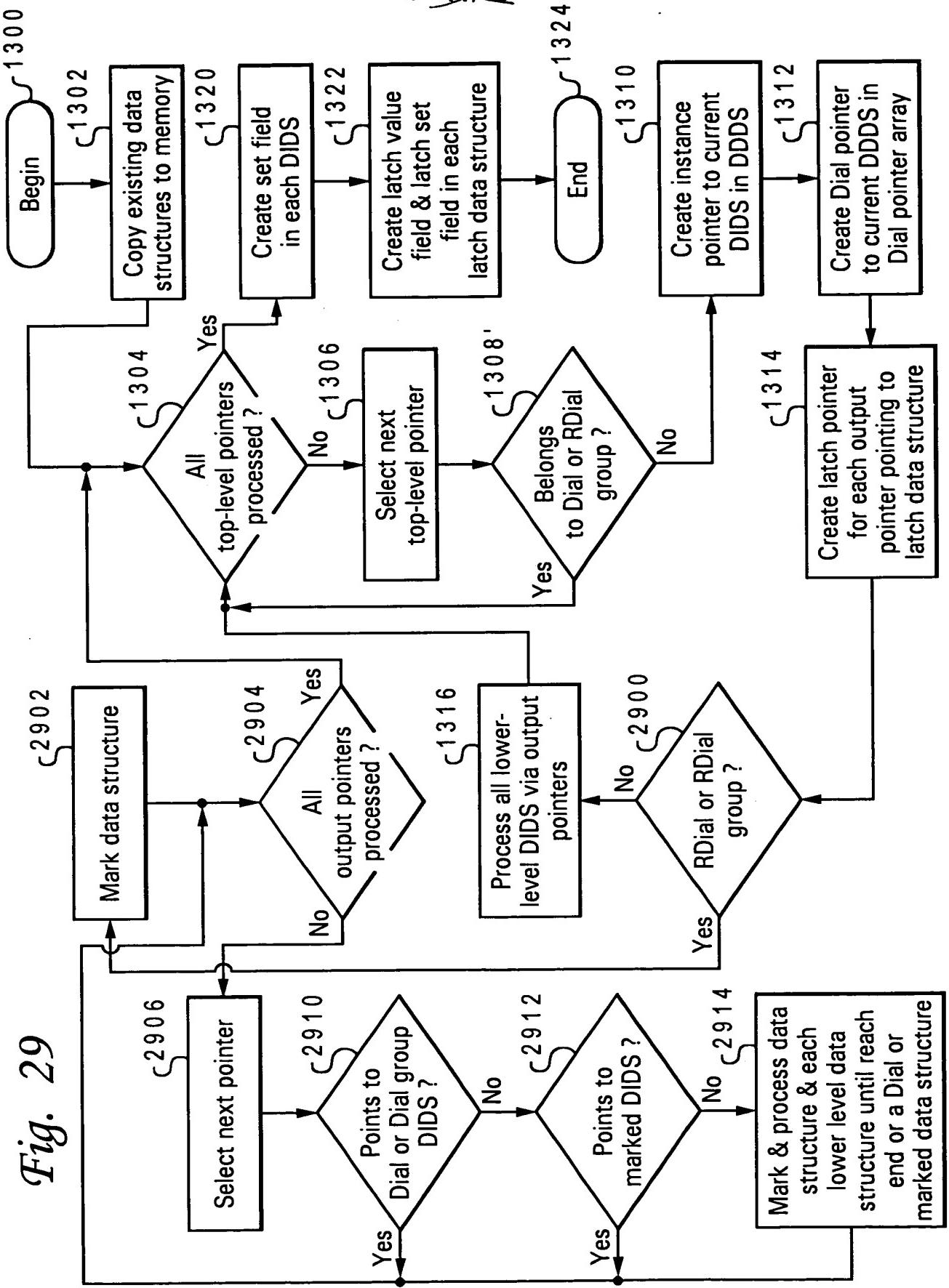


Figure 28B

Fig. 29



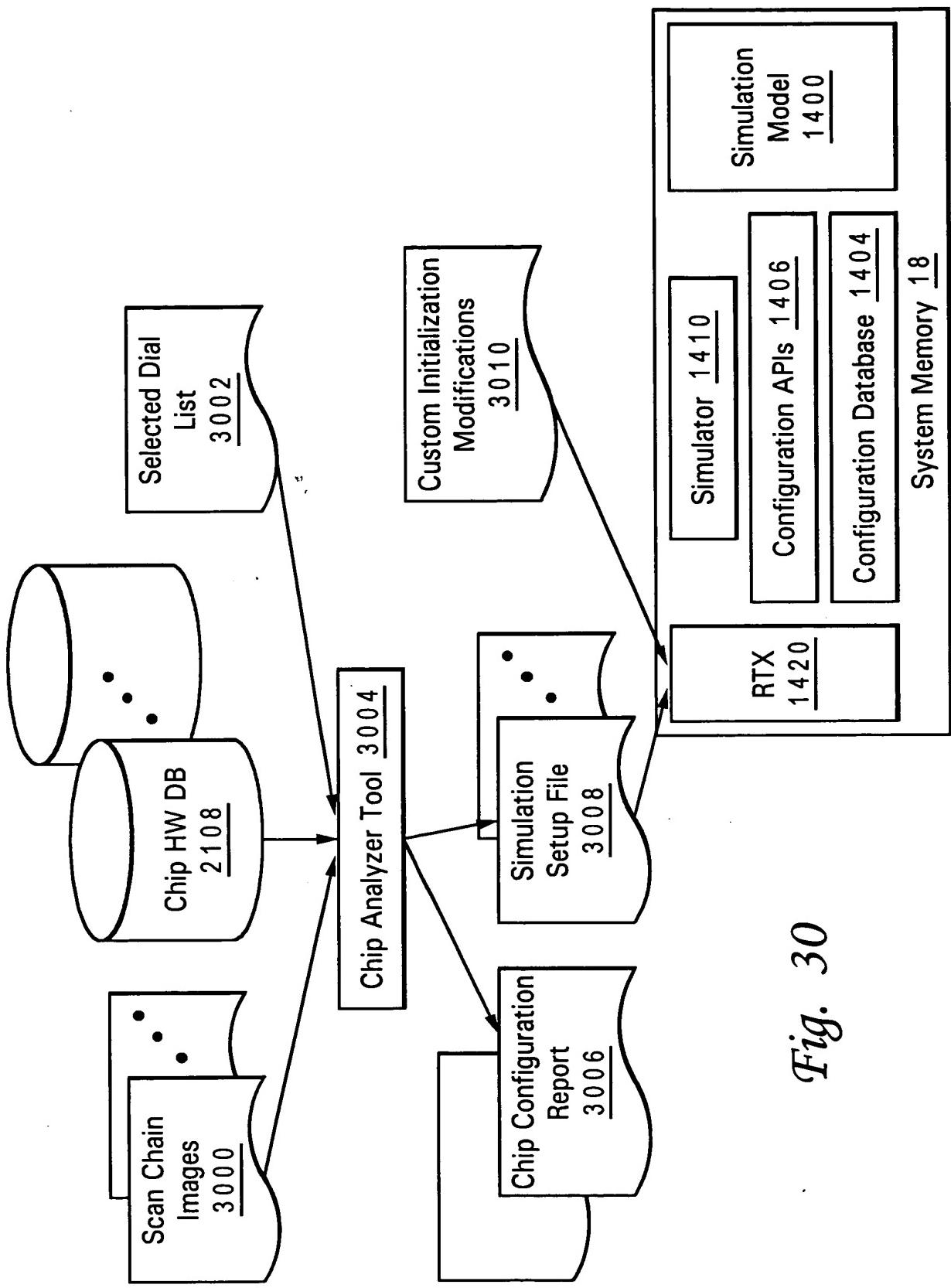


Fig. 30

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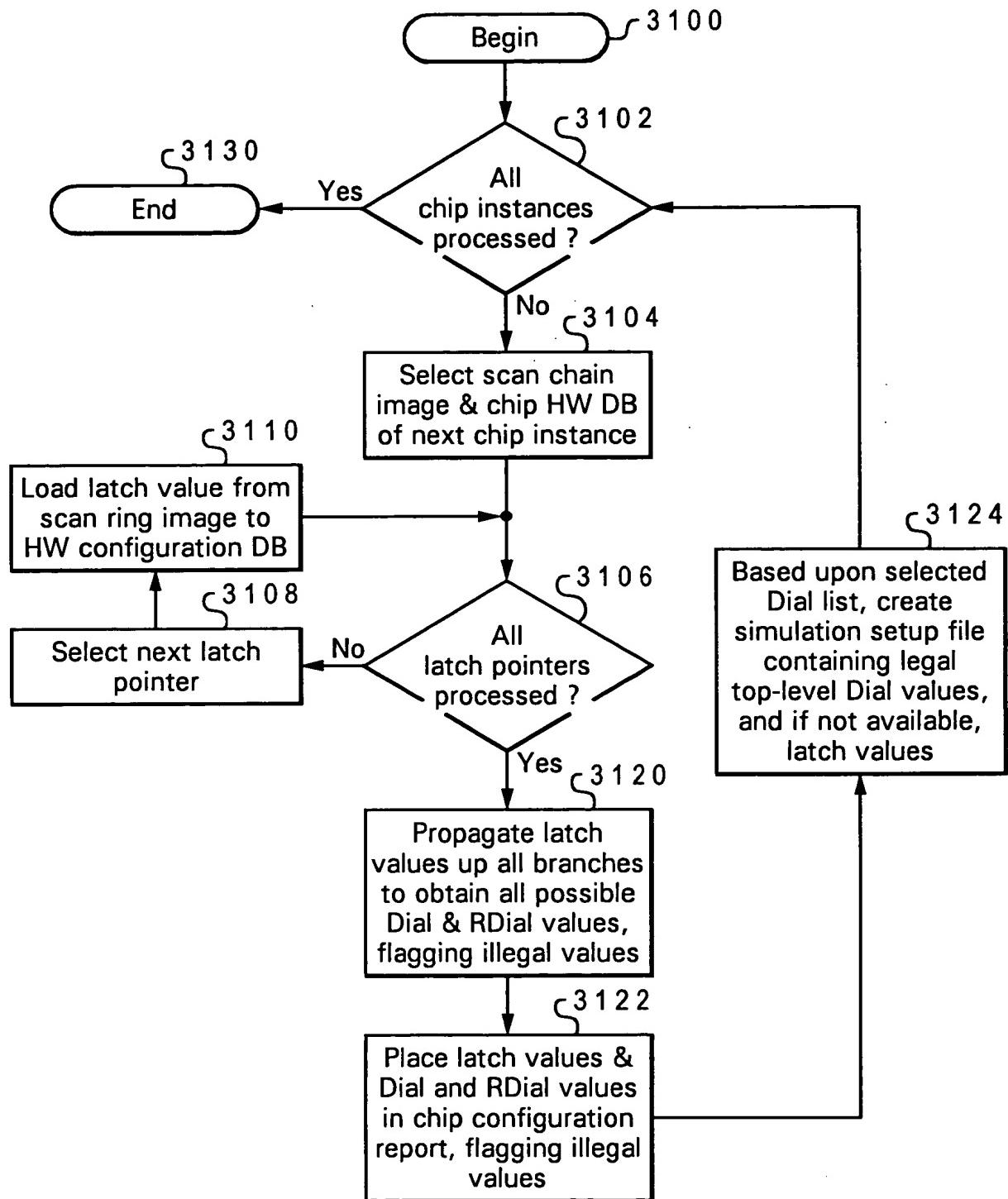


Fig. 31